

JEDEC STANDARD

JEDEC[®] Memory Controller Standard – for Compute Express Link[®] (CXL[®])

JESD319

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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JEDEC® Memory Controller Standard – for Compute Express Link® (CXL®)

(From JEDEC Board Ballot JCB-24-19, formulated under the cognizance of the JC-40.7 subcommittee on Memory Support Logic for CXL®, item number 707-99A).

A. INTRODUCTION

1 Background and Scope

This standard defines the overall specifications, interface parameters, signaling protocols, and features for a CXL® Memory Controller ASIC. The standard includes pinout information, functional description, and configuration interface. This standard, along with other Referenced Specifications, should be treated as a whole for the purposes of defining overall functionality for CXL® Memory Controller (referred to as CMC).

This standard is intended to describe a baseline of standardized functionality and pinout that is focused on the CXL 3.1 based direct attached memory expansion application. It shall not be interpreted as prohibiting any additional functionality, innovations, or other types of value-adds or customizations implementors may choose to add above the specified baseline.

The standard describes unique identification for the requirements including the baseline attributes and defaults expected for ease of reference. The unique identification ID prefixed with REQ_* are stating requirements whereas prefix OPT_* are optional features.

2 Normative References

The following normative documents contain provisions that, through reference in this text, constitute provisions of this specification. For dated or revisioned references, subsequent amendments to, or revisions of, any of these publications do not apply. Implementers are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated or unrevised references, the latest edition of the normative document referred to applies.

1. CXL Consortium. "Compute Express Link™ 2.0 Specification." CXL Consortium, Oct 2020
2. CXL Consortium. "Compute Express Link™ 3.0 Specification." CXL Consortium, Aug 2022
3. CXL Consortium. "Compute Express Link™ 3.1 Specification." CXL Consortium, Aug 2023
4. "PCI Express Base Specification Revision 5.0, Version 1.0." PCI-SIG, May 2019
5. SNIA SFF-TA-1009 Enterprise and Datacenter Standard Pin and Signal Specification, Revision 3.1
6. DMTF Security Protocol and Data Model (SPDM) Specification, Revision 1.2.0 (DSP0274)
7. DMTF Security Protocol and Data Model (SPDM) over MCTP Binding Specification, Revision 1.0.1 (DSP0275)
8. DDR4
9. DDR5
10. I3C v1.1.1
11. JESD325 "JEDEC® Memory Device Management Standard – for Compute Express Link® (CXL®)"
12. JESD317 "JEDEC® Memory Module Reference Base Standard – for Compute Express Link® (CXL®)"

3 Terms and Definitions

AIC: Add-in card. Generally accepted as a PCIe CEM adapter.

BIOS: Basic Input/Out System, modern usage synonymous with 'UEFI'

BMC: Baseboard Management Controller

CCI: Component Command Interface (CXL)

CMA: Component Measurement and Authentication (PCI-SIG)

CMC: CXL Memory Controller(JEDEC)

MM: CXL Memory Module (JEDEC). Generally accepted as a CXL Memory Device in a modularized and enclosed form factor (such as U.2, EDSFF, etc.) with embedded memory media components.

Config: Configuration

CXL: Compute Express Link

CXL Memory Device: Any CXL device advertising itself to the host as a 'CXL Memory Device' on the PCIe bus (as described in the 'Memory Device Configuration Space Layout' section of the CXL Specification). Generally accepted as any CXL Type 3 device (independent of form factor) and may include the controller, media, and other components.

DDR: Double Data Rate

DIMM: Dual Inline Memory Module

DMTF: Distributed Management Task Force

DRAM: Dynamic Random Access Memory

MC: Memory controller

PPR: Post Package Repair(JEDEC)

CRC: Cyclic Redundancy Check

Phy: Physical Interface Block

DOE: Data Object Exchange (PCI-SIG)

E1: A family of slender form factors within EDSFF (SNIA)

E3: A family of form factors within EDSFF (SNIA)

ECDSA: Elliptic Curve Digital Signature Algorithm

ECN: Engineering Change Notice

EDSFF: Enterprise and Datacenter Standard Form Factor (SNIA)

FRU: Field Replaceable Unit

FRU Information Device: Device which stores vital product data.

FW: Firmware

IDE: Integrity and Data Encryption

IPMI: Intelligent Platform Management Interface

MCTP: Management Component Transport Protocol (DMTF)

MMIO: Memory-mapped Input/Output

OOB: Out of Band

OC: Open Compute Project

OS: Operating System

PCIe: PCI Express (PCI-SIG)

PLDM: Platform Level Data Model (DMTF)

SNIA: Storage Networking Industry Association

SPD: Serial Presence Detect, modern usage referring to the device on DIMM which stores DIMM vital product data and may perform other functions such as temperature sensing.

Temp: Temperature

TS: Temperature Sensor

SPDM: Security Protocol and Data Model (DMTF)

UEFI: Unified Extensible Firmware Interface, modern usage synonymous with 'BIOS' (UEFI Forum)

VDM: Vendor Defined Message (PCI-SIG)

VPD: Vital Product Data

B. SYSTEM LEVEL DESCRIPTION

4 Overview

The CXL memory controller (referred to as Controller or CMC subsequently in the document) is intended to be used as CXL Type 3 direct-attached Memory Expander, supporting CXL.mem and CXL.io protocols. The CXL.mem protocol allows for coherent memory read/write requests from the system (CPU host), while CXL.io is used for device discovery, enumeration, error reporting, and management. The Controller integrates a CXL interface which is built upon the well-established PCI Express™ infrastructure and leverages the PCIe Gen5 physical and electrical interface to provide advanced CXL protocols. It operates at speed up to 32GT/s with optional x16 and x8 widths and can downgrade to lower speeds and widths as specified by the CXL specification. The Controller contains internal memory controller(s) which support DDR4 and DDR5 operating modes. The CXL memory requests from the system will be translated to DDR defined command/data to read/write data from/to SDRAM device or DIMM. The Controller optionally supports either one or two channels of DDR4 up to 3200 MT/s or one or two dual sub-channel DDR5 channels up to 6400 MT/s.

The Controller supports numerous security features, sideband communication, and allows for implementation specific support for internal microcontroller(s) firmware storage and secure boot and update mechanism.

The controller may be used as part of various possible topologies for CXL memory device. **Figure 1** depicts the examples.

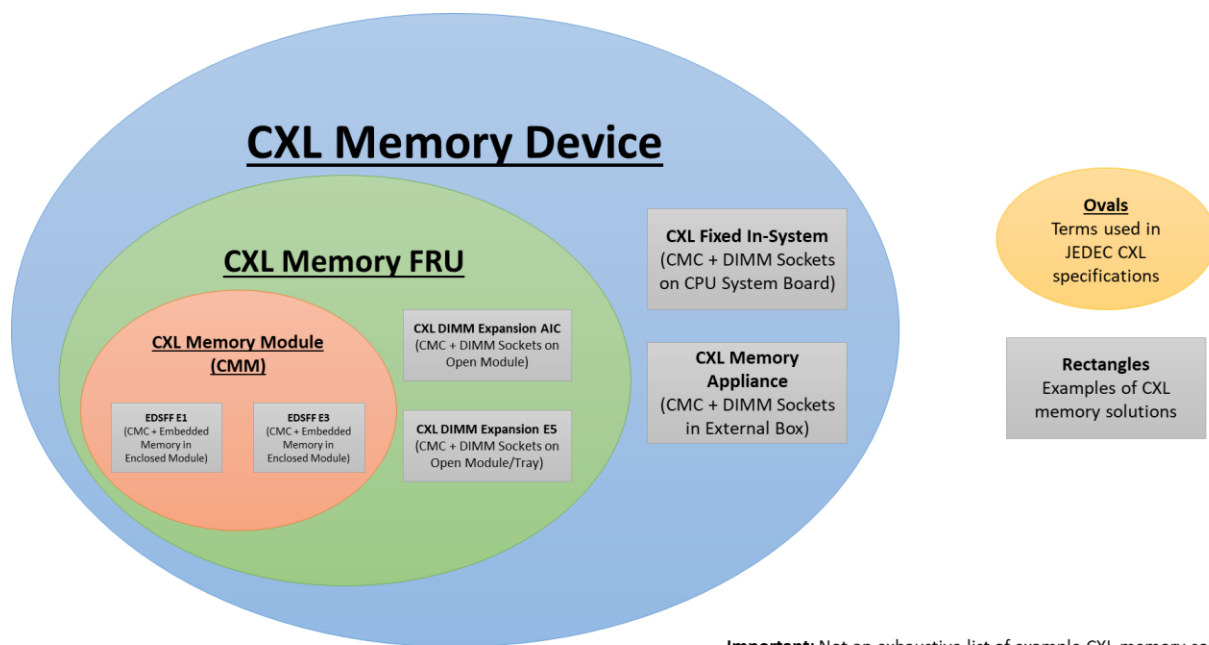


Figure 1 — CXL Memory Controller and Topologies

4.1 Implementation Options

To promote standardization across various use cases in the direct attached memory ecosystem, two different implementation options are included in the specification. Both implementations can support JEDEC compliant DDR4/5 DIMM channels, or an equivalent data width of non-DIMM attached DRAM.

4.1.1 Option #1 – X16 CXL and 2 Physical Memory Channels

The first Option shall have a X16 CXL interface that is bifurcatable into two X8 interfaces, and two physical memory channels supporting both DDR4 and DDR5 (2 physical channels of DDR4 or 2 physical channels, or 4 sub channels, or DDR5).

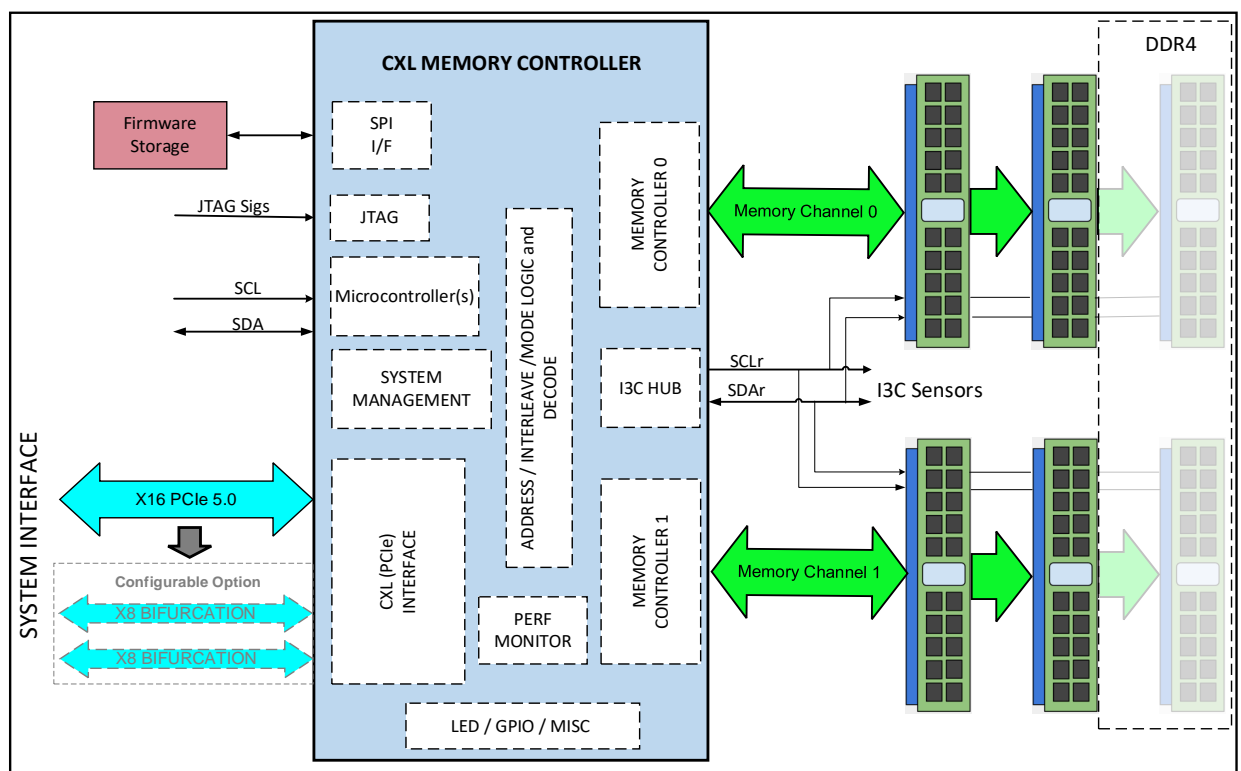


Figure 2 — High Level Block Diagram Example for Option 1, X16 2MC

4.1.2 Option #2 – X8 CXL and 1 Physical Memory Channel

The second option shall have an X8 CXL and 1 physical memory channel supporting both DDR4 and/or DDR5 (1 physical channel of DDR4 or 1 physical channel, or 2 sub-channels, or DDR5).

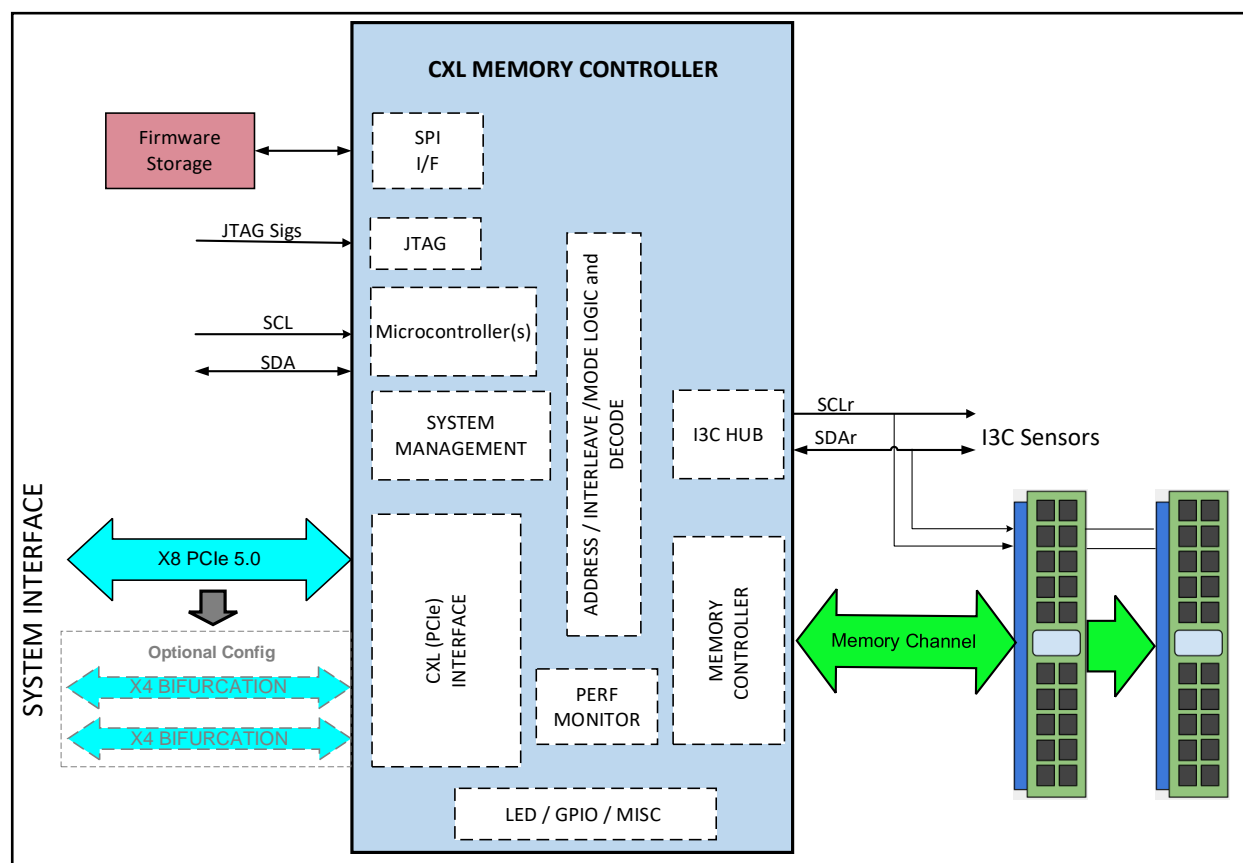


Figure 3 — High Level Block Diagram Example for Option 2, X8 1MC

4.2 Memory Support

Both DIMM and non-DIMM (e.g., soldered down DRAM) applications shall be supported. The controller shall support both X4 and X8 DRAM devices for both DDR4 and DDR5.

- DDR4 Die Support: 4Gb, 8Gb, 16Gb.
- DDR5 Die Support: 16Gb, 24Gb, 32Gb.

Table 1 indicates DRAM die support requirements and optionality as *_DIE_SUPPORT.

Table 1 — DRAM Die Support Requirements

Requirement ID	Baseline	Configurable	Default
REQ_DDR4_DIE_SUPPORT	4Gb, 8Gb, 16Gb	Yes	NA
REQ_DDR5_DIE_SUPPORT	16Gb, 24Gb, 32Gb	Yes	NA

4.2.1 DIMM Support

The controller shall support up to 2 x DDR4 or 2 x DDR5 DIMMS per physical channel as show in **Table 2**.

The UDIMM support is optional for controller but provisioned for in pinout definition.

Table 2 indicates DDR4 and DDR5 DIMM support requirements and optionality as *_DS_SUPPORT_*

Table 2 — DIMM Support Matrix

Requirement ID	Generation	DIMM Type	Physical Ranks per DIMM	DIMM per Channel	Speed Supported up to (MHz)
REQ_DDR4_DS_1	DDR4	LR/RDIMM	1-4	2	3200
REQ_DDR4_DS_2	DDR4	LR/RDIMM	1-4	2	1600
REQ_DDR5_DS_1	DDR5	RDIMM	1-2	2	6400
REQ_DDR5_DS_2	DDR5	3DS	2		6400
OPT_DDR4_DS_1	DDR4	LR/RDIMM	1-4	3 optional	1600
OPT_DDR5_DS_2	DDR5	3DS	2+		6400
OPT_UDIMM	DDR4/DDR5	UDIMM	1-4	2	As applicable

4.2.2 Discrete DRAM Support

4.2.2.1 Option 1 (2 Physical Memory Channels) Support:

- DDR5: Maximum of 160 DRAM Devices, 6400 max speed bins
- DDR4: Maximum of 144 DRAM Devices, 3200 max speed bins

4.2.2.2 Option 2 (1 Physical Memory Channel) Support:

- DDR5: Maximum of 80 DRAM Devices, 6400 max speed bins
- DDR4: Maximum of 72 DRAM Devices, 3200 max speed bins

5 Functional Description

5.1 CXL Interface

5.1.1 CXL Functionality

The Controller shall be compliant with CXL 3.1 base specification and backwards compatible to CXL2.0 and CXL 1.1. The controller's physical layer shall be compliant with PCIe Gen5 electrical specification.

The CXL memory controller device is required to support backward compatibility to CXL1.1 host by supporting either of the following methods. First and preferred implementation is MMIO registers shall be mapped into device Base Address Register (BAR) space – i.e., the non-RCRB (Root Complex Register Block). See: “Devices operating in CXL 1.1 mode with no RCRB” CXL ECN dated October 2021 for implementation. The second implementation option is supporting enumerating as Root Complex integrated endpoint, presenting the space as RCRB MEMBAR0.

5.1.2 Link Width

The CXL memory controller device specification covers two options of implementations, option1 with x16 native link width and option 2 with x8 native link width. Each option shall support degraded width including x8, x4, x2, or x1.

Additionally, the CXL memory controller device supports bifurcation capability to enable functionally independent ports. The bifurcation is enabled via pre-boot programming of <insert reference >. When the link is bifurcated, the Controller shall support following:

1. the separate links being connected to a single CPU.
2. a second CPU of a single server
3. two separate servers to enable simple pooling configurations.

Option1 shall support bifurcation ability, option2 may support bifurcation.

Each bifurcated port has the ability to function as independent port and shall support independent functioning of all CXL layers, including physical layer, link layer, transaction layer, and support degraded widths and speeds. Please refer to reset, clocking, side band section in the following document for the signaling requirements.

Implementation note: Mapping of physical lanes to the port(s) is driven based on formfactor, connector definition and is defined as part of pinout/package definition (e.g., SFF-TA-1009 Rev 3.0 table 5-2 describes mapping for dual ports for x16 and x8 dual port operation).

Footnote: The term Native refers to full bandwidth / optimal lane count operation.

The term degraded refers to operation to sub-optimal count of lanes/BW or other parameters.

5.1.2.1 Option #1

Table 3 — CXL Link Operation Modes for Option #1

Mode of Operation	Lane Configurations
X16	Native x16 (port A), degradedx8, degraded x4, degraded x2, degraded x1
Bifurcation mode x8	two individual ports with native x8 (port A and port B)
	Sub-port native x8 (port A or port B) :Native x8, degraded x4, degraded x2, degraded x1

Footnote: The term Native refers to full bandwidth / optimal lane count operation. The term degraded refers to operation to sub-optimal count of lanes/BW or other parameters.

5.1.2.2 Option #2

Table 4 — CXL Link Operation Modes for Option #2

Mode of Operation	Lane Configurations
x8	Native x8 (port A), degraded x4, degraded x2, degraded x1
Bifurcation port x4 (optional)	two individual ports with native x4 (port A and port B)
	Sub-port Native x4 (port A or port B) :Native x4, degraded x2, degraded x1

Footnote: The term Native refers to full bandwidth / optimal lane count operation.

The term degraded refers to operation to sub-optimal count of lanes/BW or other parameters.

Table 5 indicates port support requirements and optionality for option #1 (*_IF_X16_*) and option #2 (*_IF_X8).

Table 5 — CXL Interface Support Requirements

Requirement ID	Baseline	Configurable	Default
REQ_IF_x16_ports	Native x16,x8, degraded x4,x2,x1	Yes	NA
REQ_IF_x8_ports	Native x8, degraded x4,x2,x1	Yes	NA
REQ_IF_x16_Bifurcation	2 x8 native bifurcation	Yes	Disabled
OPT_IFx8_Bifurcation	2 x4 native bifurcation	Yes	Disabled

5.1.2.3 Link RAS and Security

The controller shall implement the Reliability, Availability and Serviceability requirements as specified by the CXL 3.1 specification in general, and specifically Section 12.0. In addition, the Controller shall ensure that implement the following:

- Out Of Band Error Reporting
 - Via CXL Management Interface “Component Command Interface”
 - Controller shall implement separate error records for CXL and OOB reporting and take care in design to prevent race conditions between them.
- PCIe PHY settings must be tunable to improve adaptive convergence for different channel designs. The CXL controller shall follow PCIe electrical requirements as defined by PCI Sig specification.
- Link error rate target is 1e-12 or better.

5.1.2.4 Link Integrity and Data Encryption (IDE)

The Controller may implement Link Integrity and Data Encryption (IDE) as defined by the CXL Specification Section 11.1 for CXL.mem protocol.

Table 6 — CXL IDE Support Requirement

Requirement ID	Baseline	Configurable	Default
OPT_CXL_IDE	Supported	Yes	Disabled

5.1.3 Discovery and Configuration

The Controller shall support Discovery and Configuration as specified by the CXL 3.1 specification.

5.1.3.1 Memory Capacity

The controller also shall report additional changes to capacity during initialization or run time to host system by using Memory Capacity Reduction indication in “Get Health Info: Health Status: Memory Capacity Degraded” as defined in section 8.2.9.9.3.1 of CXL specification.

Table 7 — CXL Capacity Reduction Requirements

Requirement ID	Baseline	Configurable	Default
REQ_CAP_REDN	Supported	Yes	Enabled

5.1.4 Event Logs

The Controller shall communicate Device and Media (DRAM) events to the host using the record formats and event queues defined by CXL 3.1 section 8.2.9.2. The additional details for event reporting are captured in the Event Reporting section of this specification.

5.1.4.1 Log Sizing

The following Event Logs minimum depths shall be reported via the Identify Memory Device Opcode response. The controller may support deeper log queues than depicted in **Table 8**.

Table 8 — Event Log Minimum Depths

Log Type	Minimum Depth
Informational	32
Warning	16
Failure	8
Fatal	1

Table 9 indicates event log buffer size requirements and optionality as *_LOG_SZ.

Table 9 — Log Sizing Requirements

Requirement ID	Baseline	Configurable	Default
REQ_INFO_LOG_SZ	32	Yes	Enabled
REQ_WARNING_LOG_SZ	16	Yes	Enabled
REQ_FAILURE_LOG_SZ	8	Yes	Enabled
REQ_FATAL_LOG_SZ	1	Yes	Enabled

5.1.5 CXL Device Management

The section drives commonality with CXL Memory Device Management Reference Specification JESD-325. This document enlists specific requirements from CXL controller perspective in addition to as specified in JESD-325.

5.1.5.1 SMBus/I2C/I3C Endpoint Requirements

CXL Controller supports SMBus/I2C /I3C endpoints with the following (**Table 10**):

Table 10 — Sideband Endpoint Support

SMBus/I2C Element	Default SMBus/I2C 8-bit Address	SMBus ARP Support	Required Element Presence
SMBus/I2C Management Endpoint	3Ah	Optional	Required in CXL Controller
FRU Information Endpoint	A6h	Optional	Optional in CXL Controller

Table 11 indicates management endpoint support requirements and optionality as *_EP

Table 11 — Sideband Endpoint Support Requirements

Requirement ID	Baseline	Configurable	Default
REQ_SMB_EP	Address	Yes	Enabled
REQ_FRU_Info_EP	Address	Yes	Enabled

5.1.6 CXL Mailboxes

CXL Controller shall support both primary and secondary CXL mailboxes. as described by the CXL Specification.

Note: The CXL Specification only requires a primary mailbox.

The Controller supports MMPT ECN (Management Message Pass through via MMIO Mailbox) approved by PCI SIG to enable system software management messages to pass to PCI function.

Table 12 — Mailbox Support Requirements

Requirement ID	Baseline	Configurable	Default
REQ_SEC_MAILBOX	Support secondary	Yes	Enabled

5.1.7 CXL Component Command Interface (CCI)

CXL Controller supports the CXL Component Command Interface (CCI) over the following transports:

- Primary and Secondary CXL Mailboxes as described in the CXL Specification
- MCTP as described in the DMTF CXL™ Type 3 Device Component Command Interface over MCTP Binding Specification, Revision 1.0.0. (DSP0281)

The following commands in **Table 13** shall be supported by the controller including those defined in CXL specification (specification v3.1)

(M : Mandatory; O: Optional; P: Prohibited)*

Table 13 — CXL CCI Command Support

Opcode					Required Mailbox*	Required MCTP*
Command Set Bits[15:8]		Command Bits[7:0]		Combined Opcode		
00h	Information and Status	01h	Identify	0001h	P	M
		02h	Background Operation Status	0002h	P	M
		03h	Get Response Message Limit	0003h	P	M
		04h	Set Response Message Limit Limit	0004h	P	M
		05h	Request Abort Background Operation	0005h	M	M
01h	Events	00h	Get Event Records (Section 8.2.9.1.2)	0100h	M	M
		01h	Clear Event Records (Section 8.2.9.1.3)	0101h	M	M
		02h	Get Event Interrupt Policy (Section 8.2.9.1.4)	0102h	M	P
		03h	Set Event	0103h	M	P

Opcode					Required Mailbox*	Required MCTP*
Command Set Bits[15:8]		Command Bits[7:0]		Combined Opcode		
			Interrupt Policy (Section 8.2.9.1.5)			
		04h	Get MCTP Event Interrupt Policy (Section 8.2.9.1.6)	0102h	P	M
		05h	Set MCTP Event Interrupt Policy (Section 8.2.9.1.7)	0103h	P	M
		06h	Event Notification (Section 8.2.9.2.8)	0106h	P	M
		07h	GFD Enhanced Event Notification (Section 8.2.9.2.9))	0107h	P	P
		08h	GFD to GAE Enhanced Event Notification (Section 8.2.9.2.10)	0108h	P	P
		09h	Get GAM Buffer (Section 8.2.9.2.11)	0109h	P	P
		0Ah	Set GAM Buffer (Section 8.2.9.2.12)	010Ah	P	P
02h	Firmware Update	00h	Get FW Info (Section 8.2.9.3.1)	0200h	M	M
		01h	Transfer FW (Section 8.2.9.3.2)	0201h	M	M
		02h	Activate FW (Section 8.2.9.3.3)	0202h	M	M

Opcode					Required Mailbox*	Required MCTP*
Command Set Bits[15:8]		Command Bits[7:0]		Combined Opcode		
03h	Timestamp	00h	Get Timestamp (Section 8.2.9.4.1)	0300h	M	M
		01h	Set Timestamp (Section 8.2.9.4.2)	0301h	M	M
04h	Logs	00h	Get Supported Logs (Section 8.2.9.5.1)	0400h	M	M
		01h	Get Log((Section 8.2.9.5.2)	0401h	M	M
		02h	Get Log Capabilities (Section 8.2.9.5.3)	0402h	O	O
		03h	Clear Log (Section 8.2.9.5.4)	0403h	M	M
05h	Features	00h	Get Supported Features (Section 8.2.9.6.1)	0500h	M	M
		01h	Get Feature (Section 8.2.9.6.2)	0501h	M	M
		02h	Set Feature (Section 8.2.9.6.3)	0502h	M	M
06h	Maintenance	00h	Perform Maintenance (Section 8.2.9.7.1)	0600h	M	M

5.2 Memory Controllers

5.2.1 Page Policy Support

The memory controllers shall support Open, Closed, and a vendor defined Adaptive paging policy. The policy is set via the *Page_Policy* field of the *Page Policy and Interleave Mode* configuration, described in **Controller Configuration**.

5.2.1.1 Closed Page Policy

Accessed page is “closed” and pre-charged immediately after a read or write access. When the Page_policy is set to closed page policy, the CXL controller shall issue RDA or WRA (commands with Auto-Precharge) instead of RD or WR as per DDR4/DDR5 command truth table.

5.2.1.2 Open Page Policy

Access page is left “open” for a fixed interval after a read or write transaction. The page open interval is configurable via the *Page Policy and Interleave Mode* configuration. If the access pattern requires the controller to open another page from the same bank, the controller shall close the page ‘left’ open before opening a new page.

5.2.1.3 Optional - Adaptive Open Page Policy

Access page is left “open” for a variable period based on access pattern heuristics. The intent is that the page open interval is adapted based on recent page hit/miss statistics and power/performance requirements. Implementation is vendor specific and may have additional configuration settings.

Table 14 indicates page policy support requirements and optionality as *_<policy>

Table 14 — Page Policy Requirements

Requirement ID	Baseline	Configurable	Default
REQ_Open_page	Open Page policy supported	Yes	Disabled
REQ_Closed_page	Closed Page policy supported	Yes	Enabled
OPT_Adaptive_page	Adaptive Page policy supported	Yes	NA

5.2.2 Interleave Modes

The memory controllers shall support the following Device Physical Address interleave modes across the DRAM controllers. This mode is configured via the *Page Policy and Interleave Mode* configuration. All modes have a baseline interleave granularity of 256B supported as default to match the CXL interleave minimum granularity. In addition, the controller shall support configurable interleave granularity(IG) for 64B, 256B, and 1024B, selectable via configuration, described in **Controller Configuration**.

5.2.2.1 Interleaved Address Mapping

Table 15 — Interleave Address Mapping

								Mode (Recommended Use)
	An.....DPA[n:0].....A0							
X	Channel	Rank	Bank Group	Bank	Row	Column	IG	Linear
X	Row	Rank	Bank	Bank Group	Channel	Column	IG	Open Page
X	Row	Column	Rank	Bank	Bank Group	Channel	IG	Closed Page
CID	Row	Rank	Bank	Bank Group	Channel	Column	IG	3DS Open Page
CID	Row	Column	Rank	Bank	Bank Group	Channel	IG	3DS Closed Page
								Vendor Defined Config 1
								Vendor Defined Config 2

The Controller may additionally support one or more vendor defined interleave schemes.

Table 16 indicates address interleaving mode support requirements and optionality as *_INTLV_*.

Table 16 — Address Interleaving Requirements

Requirement ID	Baseline	Configurable	Default
REQ_INTLV_MODE_1	Linear interleave	Yes	Disabled
REQ_INTLV_MODE_2	Open Page	Yes	Disabled
REQ_INTLV_MODE_3	Closed Page	Yes	Enabled
OPT_INTLV_MODE_1	3DS open page	Yes	Disabled
OPT_INTLV_MODE_2	3DS Closed page	yes	Disabled

5.2.3 Device Physical Address

The device physical address is mapped to the device stuffed DRAM capacity in one of three ways determined by the number of configured CXL ports, Address Mode:

5.2.3.1 Single Port

In this configuration the DPA is mapped onto the full aggregate memory capacity based on the Interleave mode.

5.2.3.2 Dual Port - Divided

The configuration is applicable when the Controller is configured with dual CXL ports (bifurcated) the memory capacity is divided by splitting the available DRAM channels between the ports. (Each CXL Port may connect to individual CPUs on a single server, or CPUs on different servers).

Table 17 — Dual Port Divided Mode DRAM Channel Mapping

		Port 0	Port 1
DDR4	Channel 0	X	
	Channel 1		X
DDR5 1-Channel	Sub-Chan 0	X	
	Sub-Chan 1		x
DDR5 2-Channel	Sub-Chan 0	X	
	Sub-Chan 1	X	
	Sub-Chan 2		X
	Sub-Chan 3		X

Performance in this mode should be balanced between ports – both in bandwidth, and in bandwidth/GB memory.

5.2.3.3 Dual Port – Sectioned

In this mode, the aggregate attached memory capacity is divided between two CXL ports. This mode and the address boundary are set by the *Physical Address Configuration*, described in the **Controller Configuration**.

Address_Boundary = Sectioned_Address (register field) * 256B

Port 0 Capacity = Address_Boundary.

Port 1 Capacity = Device_Capacity - Address_Boundary.

5.2.3.3 Dual Port – Sectioned (cont’d)

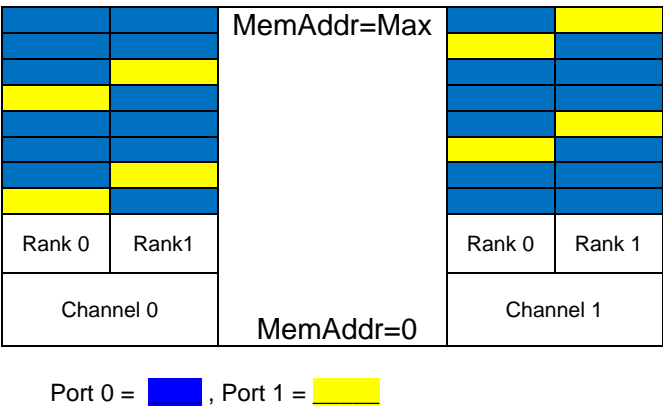


Figure 4 — Example Dual CXL Port Address Mapping

In the simplified example of **Figure 4**, Port-0 is configured to have 3/4th of the device capacity and Port-1 1/4th of the capacity. Note that both Port-0 and Port-1 are interleaved across all channels and ranks (set by the interleave mode).

Performance between cxl ports in this mode is generally balanced and limited by the bifurcated CXL link. Note this can create an asymmetry in bandwidth/GB of memory. Implementers may add additional QoS capabilities as needed.

Table 18 indicates dual port address mapping support requirements and optionality as **_DP_**.

Table 18 — Dual Port Addressing Requirements

Requirement ID	Baseline	Configurable	Default
REQ_DP_DIVIDED	Uniform division of address space across ports	Yes	Enabled
REQ_DP_SECTIONED	Sectioned division of address space	Yes	Disabled

5.3 Memory RAS and Metadata

5.3.1 DRAM ECC

The Controller shall support ECC functionality on each of the external DRAM channels for both DDR4 and DDR5 operation. A minimum of two ECC levels are supported – to be able to detect and correct single bit errors and multi-bit errors in a single DRAM device(as applicable). Additionally, chipkill functionality, i.e., ability to correct multi-bit errors within the same DRAM device, is supported when used with X4 DRAM devices, as well as Bounded Fault (BF) functionality with X8 devices.

A possible example for such implementation is the SECDED and RS-36-32-8 , however they are included here as specific reference implementations, the specification is not intended to prevent an implementer from using a different algorithm or methodology if its minimum ECC capability is at least equivalent to these described levels.

Table 19 — ECC Support by DIMM Type

	DDR4 X4 DRAM	DDR4 X8 DRAM	DDR5 X4 DRAM	DDR5 X8 DRAM	DDR5 9x4 DIMM
ECC(ex SECDED)	Yes	Yes	Yes	Yes	Yes
“Chipkill”(ex RS-36-32-8)	Yes	-	Yes	-	-
Bounded Fault	NA	NA	NA	Yes	Yes

5.3.1.1 Configuration and Basic Operation

If ECC is enabled in the parameter defined in feature, the Controller ECC logic performs the following functions:

- On writes, the ECC is calculated across each ECC lane, and the resulting ECC code is written as described in the mode specific sections below.
- On reads, the ECC lane including the ECC data is read from DRAM. It is then “decoded”, and a check is performed to verify data correctness using the parity/check information . If it is correct, the data is sent to the Host as normal.
- On read-modify-write (RMW) operations, a read is first performed and ECC check is completed, then the read data is then combined with the write data received from the System, making use of any write mask received as well to over-write certain bytes of the read data. The ECC is then calculated on the resulting word, and a write back to the DRAM is executed.

5.3.1.2 Controller Behavior During ECC Errors

If the read is issued to location which has previously stored poison bit, the controller shall ignore the data and return poison to the host transaction.

Correctable Error:

1. Corrects the error and returns the corrected data in response to the Host read command. In addition, if Demand Scrubbing is enabled (Section 5.3.2.2), the corrected data is written back to the original DRAM address.
2. Error event logging section covers the error event record details.

Uncorrectable Error:

1. Responds to the read request with the uncorrected data plus a Poison status.
2. Error event logging section covers the error event record details.
3. If the configuration setting as defined in error event reporting section is enabled the controller shall write the poison back to memory location while intentionally corrupting the data

In addition to the previous uncorrectable behavior, when the DRAM Controller detects an uncorrectable error during the read part of a normal RMW command, it does the following:

- During the subsequent write part of the normal RMW command, it performs an uncorrectable corruption to the recalculated ECC parity or check bits and/or writes the poison bit based on configuration setting.

5.3.1.3 Implementation Note

The following clauses describe reference algorithms for minimum ECC capabilities using SECDED mode and RS-36-32-8 mode.

5.3.1.4 SECDED Mode

The memory controller may choose to support SECDED mode in the configurations described below. The SECDED functionality shall be implemented as a Hamming code with 7 parity bits to provide Single Bit Correction, plus an additional all-data-bit parity for Double Bit Detection.

5.3.1.4 SECDED Mode (cont'd)

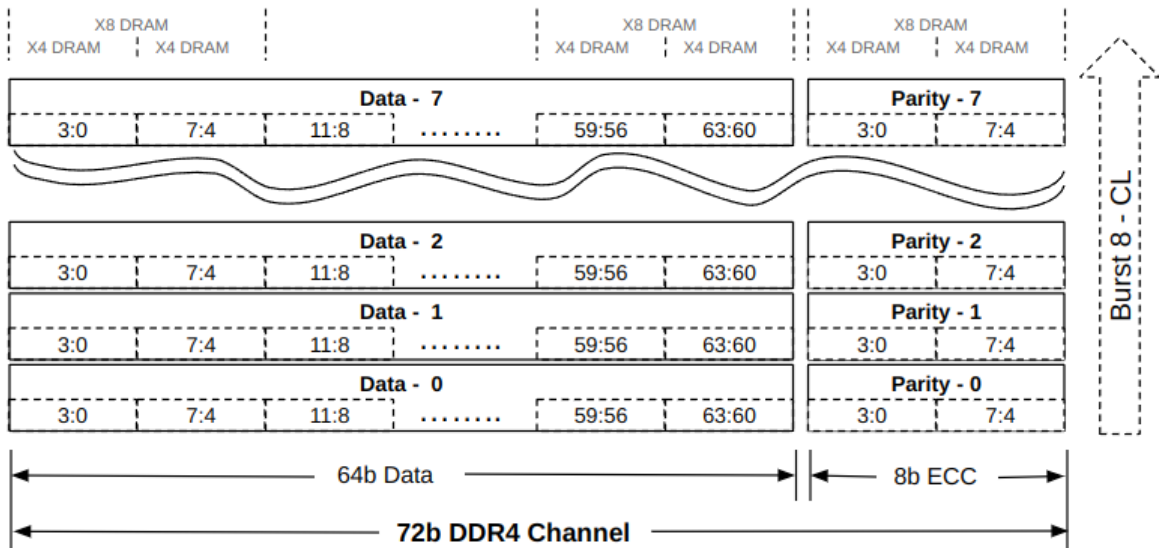


Figure 5 — DDR4 SECDED ECC Codeword Assignment

In this configuration, one “beat” of the DRAM data, 64 bits total, is used to create the 8 Parity check bits. The bits are written to and contacted in the most-significant byte of the 72b DRAM bus data. X4 and X8 DRAM devices are supported equally in this mode.

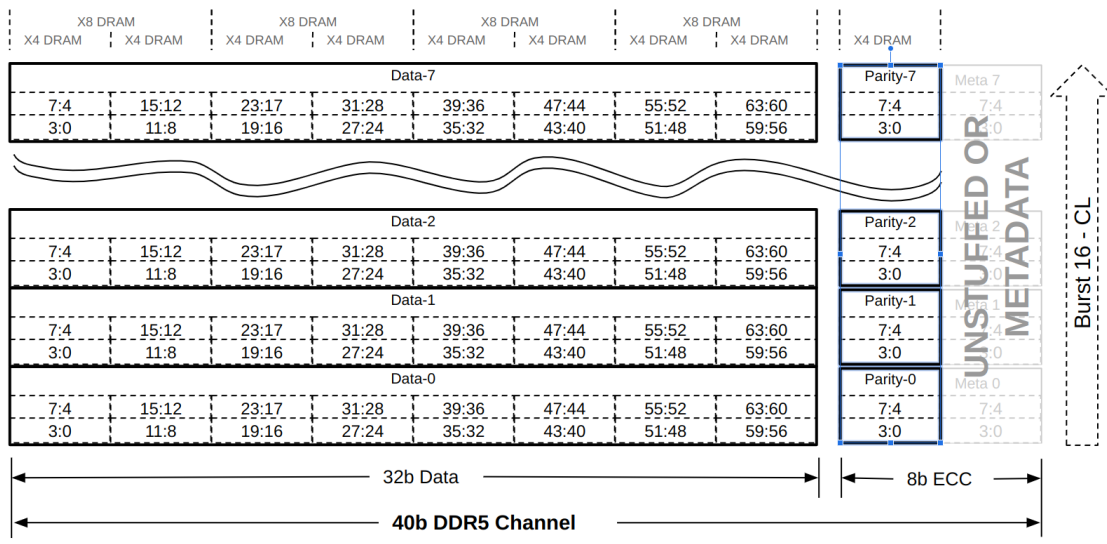


Figure 6 — DDR5 SECDED ECC Codeword Assignment

In this configuration, two “beats” of the DRAM data, 64 bits total, are used to create the 8 Parity check bits. The 8 bits are written to and stored in consecutive locations on the 9th most-significant nibble of the 80b DRAM bus. X4 and X8 DRAM devices are supported equally in this mode.

Note that this mode supports 5x8b, 10x4b, and 9x4b DIMM configurations. In 5x8b and 10x4b configurations, the most significant nibble of the 80b DRAM bus is unused for ECC and is available for implementation specific Metadata uses.

5.3.1.5 RS-36-32-8 Mode

5.3.1.5.1 Overview of RS-36-32-8 ECC Mode

The RS-36-32-8 ECC mode uses symbol-based Reed-Solomon encoding. The code is specified with the notation RS (36, 32, 8), where one symbol is 8 bits, message (data) length is 32 symbols (256 bits), ECC parity length is 4 symbols (32 bits), and the code word (data and ECC) length are 36 symbols (288 bits). This RS code can correct up to 2 symbol errors. Correction and/or detection in the case of more than 2 symbol errors is uncertain due to aliasing effects.

A symbol error is defined as any erroneous bit combination within one symbol.

Note that an aliasing effect can result when the number of symbol errors are more than 2. If the number of symbol errors are either 3 or 4, the aliasing effect can happen during correction. If the number of symbol errors is more than 4, then aliasing can happen during detection and correction.

On writes, the Reed-Solomon Encoder (RSE) calculates an ECC code word across each group of 32 symbols, generating a 36-symbol code word. On reads, the Reed-Solomon Decoder (RSD) decodes the data and ECC data then checks for symbol errors.

In all DIMM/DRAM configurations, the Symbol and Check bits are assigned to maximize their effectiveness given anticipated failure mechanisms. Specifically, these are assigned to allow “stuck-at faults” on any one data/check bit to only corrupt one symbol, reserving one symbol correction for additional bit errors. The symbols are also assigned such the “Chipkill” - the ability to correct for a complete device failure – is enabled on a nibble boundary. This supports the feature for X4 devices, as well as Bounded Fault functionality with X8 devices.

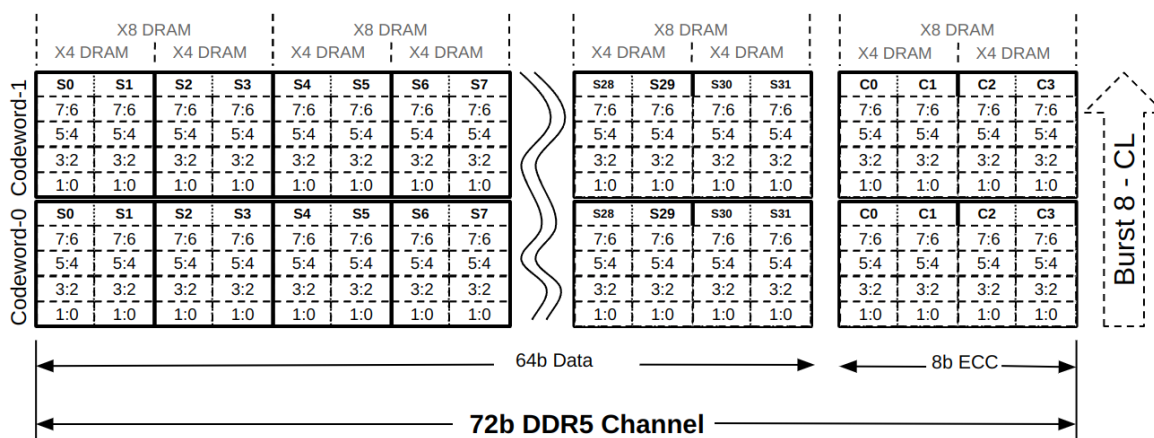


Figure 7 — DDR4 Reed Solomon ECC Codeword Assignment

In this configuration, four “beats” of the DRAM data, 256 bits total, are used to create the 4 Parity check bytes. The 4 Check bytes are written to and stored in consecutive locations of the most significant byte of the 72b DRAM bus. X4 and X8 DRAM devices are supported equally in this mode; however, Chipkill functionality is only supported when X4 DRAM are used.

5.3.1.5.1 Overview of RS-36-32-8 ECC Mode (cont'd)

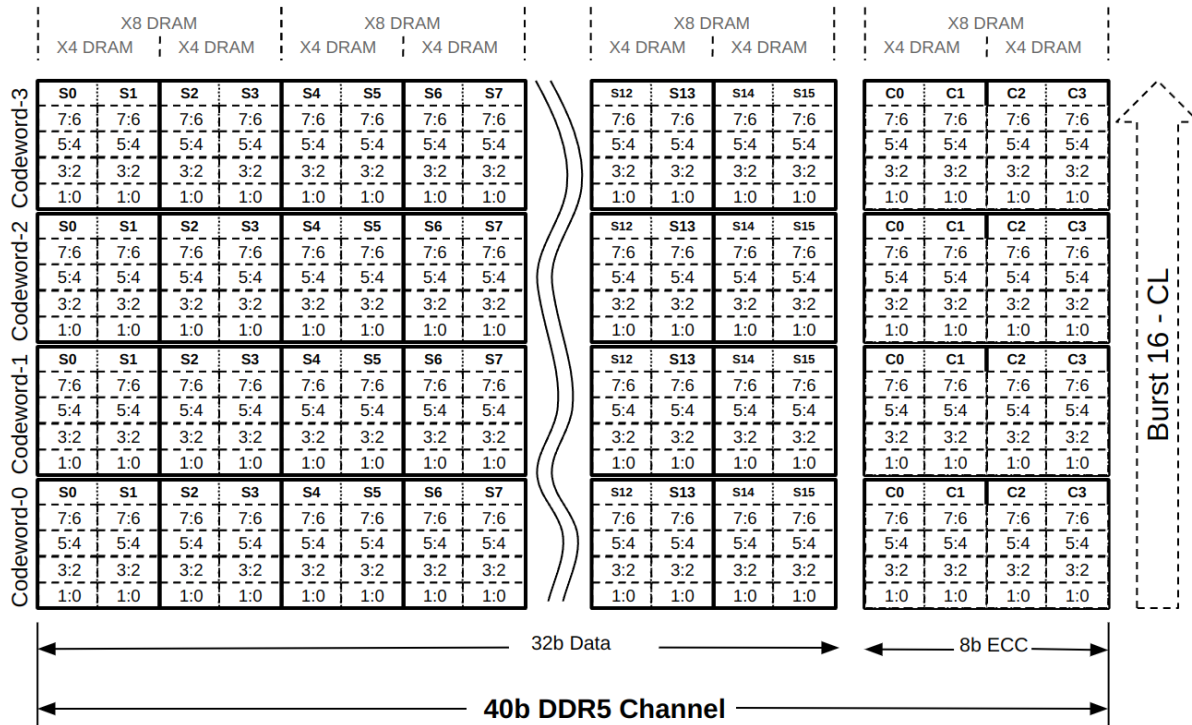


Figure 8 — DDR5 Reed Solomon ECC Codeword Assignment

In this configuration, four “beats” of the DRAM data, 128 bits total, plus 128b of “zero” padding data are combined into the 256b that are used to create the 4 Parity check bytes. The 4 Check bytes are written to and stored in consecutive locations of the most significant byte of the 40b DRAM bus. X4 and X8 DRAM devices are supported equally in this mode; however, Chipkill functionality is only supported when X4 DRAM are used; however, X8 devices with Bounded Fault designs are also supported.

Notes:

- Symbol error is defined as any erroneous bit combination within one symbol.
- An aliasing effect can result when the number of symbol errors is more than 2. If the number of symbol errors are either 3 or 4, the aliasing effect can happen during correction. If the number of symbol errors is more than 4, then aliasing can happen during detection and correction.

On writes, the Reed-Solomon Encoder (RSE) calculates an ECC code word across each group of 32 symbols, generating a 36-symbol code word. These four bytes of ECC data are always written to the uppermost byte of SDRAM (byte 4 for a 32-bit DRAM DDR5 sub-channel, or byte 8 for 64-bit DRAM DDR4 channel).

On reads, the Reed-Solomon Decoder (RSD) decodes the data and ECC data then checks for symbol errors. If the data is correct, it is sent to the requestor as normal. If a symbol error is detected, the behavior is the same as SECDED ECC mode.

5.3.2 Patrol and Demand Scrubbing

5.3.2.1 Patrol Scrubbing

CXL memory Controller supports patrol scrubbing mechanism. If enabled, Patrol scrubbing will cycle through the entire configured DRAM capacity, reading each location, correcting errors if possible and then writing the corrected values back to the DRAM. The scrub interval (period to make one complete pass through memory) shall be configurable via Device Patrol Scrub Control feature as defined in CXL 3.1 specification section 8.2.9.9.11 (Media Device Features). The default setting for patrol scrub shall be programmed by controller in a way that entire memory address range is scrubbed at least once in 24 hours period. All correctable and uncorrectable memory errors handled as described in the 5.12. The controller shall report patrol scrub errors in real time and indicate so via “Patrol Scrub Real-time Reporting Capable” bit in Device Patrol Scrub Feature Control.

5.3.2.2 Demand Scrubbing

The controller supports configurable demand scrubbing mechanism. If demand Scrubbing is enabled, the Memory Controller will write back the corrected value to the DRAM after a demand read that resulted in a correction.

5.3.3 ALERT# Behavior

The ALERT# signal is dual-use and can signal either a Write CRC or CA Parity Error to the controller. Immediately upon ALERT# assertion, the Memory Controller shall stop issuing new DRAM commands and shall service the signaled error condition.

CA Parity and Write CRC errors are differentiated by the width of the ALERT# assertion (see DDR and RCD specifications) and the controller implementation should be able to differentiate these conditions – with the CA Parity being signaled by a substantially longer duration ALERT# assertion. Note that a special condition exists where multiple Write CRC's may happen back-to-back, producing an aggregate ALERT# (assertions OR'd logically on modules) that can be mistaken for a CA parity error. Controller logic should poll the DRAM MR53 Write CR status bits to differentiate the conditions.

5.3.4 Write CRC and Retry

Write CRC functionality as defined in the JEDEC DDR4 and DDR5 specifications is supported. Write CRC errors are signaled by the dual-use ALERT# signal. Care should be taken to ensure that the maximum ALERT# latency is accounted for in implementing a write retry buffer. Specific implementations may choose between a replay of all writes during the potential error window, or DRAM Rank MR50 registers may be polled to determine a subset of writes to be replayed.

Write CRC Retry functionality shall be enabled and configured as described in **Controller Configuration**.

5.3.4 Write CRC and Retry (cont'd)

The Retry Status flag indicates the Memory Controller has detected a Write CRC Condition and is in the process of replaying the applicable write commands (the Retry). This flag is cleared if the Retry was accomplished without additional Write CRC errors. The Retry of buffered writes is redone if there is a Write CRC error during the current retry attempt. This is repeated a maximum number of times, as set by the Max Retries field and is tracked by a retry counter. A Fatal Error is logged if the Max retry count is reached before the Retry is successful.

If the Retry is successful, the retry counter is reset to zero, the Retry Status is cleared and subsequent DRAM commands that were held and queued due to the ALERT assertion detection may be completed.

5.3.5 CA Parity and Retry

The Memory Controller supports retry for Command Address Parity Retry (CA parity retry) In both DDR4 and DDR5 modes, if supported in the topology/configuration. The parity check is done by the RCD and/or SDRAM depending on protocol and configuration of the memory.

CA parity check is supported by the RCD for DDR5/4 and SDRAM for DDR4. A CA Parity error is signaled to the DRAM via the dual-use ALERT# signal.

Table 20 — CA Parity Configurations

CA Parity Retry Check		
Protocol	Parity Check is Done by	Automatic Retry by the Controller
DDR4	SDRAM	Supported
DDR4	RCD ((L)RDIMM)	Supported
DDR5	RCD ((L)RDIMM)	Supported

CA Parity Retry is enabled via the *Write CRC and Parity Configuration*.

In the cases where CXL controller doesn't support CA parity function, i.e., DDR5 without RCD, the controller shall support configurable 2N mode for CA pins.

5.3.5.1 CA Parity Error Handling

The sequence for handling CA Parity Errors is defined in the applicable JEDEC DRAM and RCD Specifications. If CA Parity Retry is not enabled and CA Parity Error is detected, a fatal error event is logged. If CA parity retry is enabled, the controller shall enable a programmable threshold for retry attempts, and failure beyond the threshold shall log fatal CA parity event as described in **Error Reporting and Handling**. The programmable threshold is included as part of **Controller Configuration**.

5.3.5.2 CA Parity Retry Limit

The Memory Controller shall support two types of CA Parity error limits:

1. **Retry Limit:** A configurable limit on the maximum number of consecutive retries before the CA Parity condition is cleared.
2. **Max Errors:** A configurable limit on the maximum number of CA Parity errors detected before the CA Parity error is reset.

The CA retry modes and thresholds are configured via the *Write CRC and Parity Configuration*, described in the **Controller Configuration**.

5.3.6 Read CRC and Uncorrectable Memory ECC Errors

Read CRC is supported in DDR5 DRAMs. When enabled, the DRAM generates a CRC checksum of the read data and then transmits this data and checksum to the Memory Controller. The Memory Controller then compares the received checksum against its computed checksum of the data. If the two checksums do not match, DRAM Controller retries the suspect read transaction when Read CRC Retry function is enabled.

5.3.6.1 Read Retry and Uncorrectable Memory ECC Errors

This section applies to Read CRC and Memory Uncorrectable ECC Errors.

Host read commands are stored in a Retry command buffer. When read data returns from the DRAM and the Memory Controller detects either a Read CRC or uncorrectable (UC) ECC error, if the associated retry functionality is enabled, the Memory Controller discards the burst of corrupted read data and re-executes the failing read command again.

If the re-read data is free from errors, the data shall be sent to the host in response to the original read command.

If the re-read data still has either a Read CRC or UC ECC error, the read may be retried up to a configurable number of times, the MAX_READ_RETRIES. If the max retries limit is reached, the event is logged in the event record, as referenced in Error Event reporting section, and the read data is returned POISONED in response to the original read request.

If CRC Read Retry is not enabled, and a Read CRC error occurs, the event is logged in event record, as referenced in Error Event reporting section, and the read data is returned POISONED in response to the original read request.

If UC ECC Error Retry is not enabled, and an UC ECC Error occurs, the event is logged in the event record, as referenced in Error Event reporting section, and the read data is returned POISONED in response to the original read request.

UC ECC errors shall be ignored in the presence of Read CRC errors. In the case of a RMW, the read-retry functionality from above is applied to the read portion of the RMW.

See Section Errors for log details.

Read CRC Retry, UC ECC Retry, and MAX_READ_RETRIES are configurable via the configuration setup, described in the **Controller Configuration**.

5.3.7 sPPR and hPPR

The controller shall support the Maintenance commands as defined in CXL3.1 (section 8.2.9.7), and is enabled to provide sPPR (runtime and boot time) and hPPR functionality. The controller supports device initiated and host initiated sPPR/hPPR operations.

Note: Runtime PPR refers to data being preserved during the operation. CXL controller reports the capability to retain the data during sPPR operation via “Restriction flags” bit in feature payload, as defined in CXL specification.

5.3.8 Memory Sparing

If controller supports memory sparing related capabilities (optional) , controller shall use CXL defined interface to describe memory sparing capabilities and configuration via Maintenance Operation.

5.3.9 Error Injection

The Controller shall support Poison Injection in compliance with CXL 2.0 “Compliance ECN – Memory Device Error Injection”, Section 14.16.4.17.

5.3.10 Metadata Support

The Controller may optionally support the storage, read, and write of Metadata to the DRAM. In this context, Metadata is additional information stored in DRAM that is intended to encode Meta state and is used in conjunction with the MetaField and MetaValue Fields of Requests/Responses.

The Controller may include additional DRAM ECC modes beyond the minimal required mode that allow for the trade-off of ECC for metadata storage. Care should be taken to ensure that Metadata is included in the ECC detection/correction coverage.

Table 21 indicates memory controller RAS requirements and optionality as *_<feature_name>

Table 21 — Memory Controller RAS Requirements

Requirement ID	Baseline	Configurable	Default
REQ_DRAM_ECC	Supported	Yes	Enabled
REQ_SDDC	Supported for specific DRAM config	Yes	Disabled
REQ_DRAM_BF	Supported for specific DRAM config	Yes	Disabled
REQ_PSCRUB	Supported	Yes	Enabled
REQ_DEMAND_SCRUB	Supported	Yes	Enabled
REQ_WRCRC	Supported	Yes	Disabled
REQ_RDCRC	Supported	Yes	Disabled
OPT_SPARING	NA	Yes	Disabled
REQ_sPPR	Supported (Host initiated, Dev initiated)	Yes	Dev Initiated
REQ_hPPR	Supported (Host initiated, Dev initiated)	Yes	Dev Initiated
REQ_ERR_INJ	Supported	Yes	Enabled
OPT_METADATA	Optional	Yes	Disabled
REQ_CA_PARITY	Supported for specific DIMM topology	Yes	Enabled

5.4 Data Integrity Risk Mitigations

The controller shall support data integrity functions such as DRFM/RFM/PRAC as applicable to the technology being supported per JEDEC spec requirements to ensure RAS.

Table 22 — Data Integrity Risk Mitigation Requirements

Requirement ID	Baseline	Configurable	Default
REQ_DRFM	Supported(as per technology supported)	Yes	Enabled
REQ_PRAC	Supported (as per technology supported)	Yes	Enabled

5.5 DRAM MBIST

The controller shall support the Device Built-In test operations function as described in CXL 3.1 section 8.2.9.7.1.5 for host/system-initiated media testing. The controller shall publish Media Test Capability Log Entry for each of the supported tests. The controller shall support following algorithms:

01h: Write , Read and Compare Patterns

02h: Checkerboard

03h: MARCH

04h: MATS

05h: MATS+

06h: Walking 1's

07h: Walking 0's

The controller may additionally support vendor defined algorithm and vendor defined pattern. The controller shall support configurable address range and indicate it to the host via Address Configurable Flag bit in the Media Test capability entry. In addition, the controller shall support “Inverse Patter Support”, “Exit on Uncorrectable Error”, and “Addressing Mode”. In event of error encountered during the test, the controller shall populate Media Test Results Short Log and Long Log including the error signature(s). The controller shall support at least 8 error signatures to be reported.

In addition, controller shall support “Data and Metadata ECC Disablement Capability” and “Metadata Area Testing Capability”.

In addition, the controller shall support media testing during initialization and training sequence independent of system initiation.

If the sPPR operation mode (see section 5.3.7) is set to “Device Initiated”, the device firmware shall monitor the errors detected during Device Built-In test operations and shall initiate sPPR actions as needed.

Table 23 indicates Memory testing algorithm support requirements and optionality as *_MBIST_<algorithm>.

5.5 DRAM MBIST (cont'd)

Table 23 — Memory Testing Requirements

Requirement ID	Baseline	Configurable	Default
REQ_MBIST_01	Supported(Algorithm ID= REQ_ID)	Yes	NA
REQ_MBIST_02	Supported(Algorithm ID= REQ_ID)	Yes	NA
REQ_MBIST_03	Supported(Algorithm ID= REQ_ID)	Yes	NA
REQ_MBIST_04	Supported(Algorithm ID= REQ_ID)	Yes	NA
REQ_MBIST_05	Supported(Algorithm ID= REQ_ID)	Yes	NA
REQ_MBIST_06	Supported(Algorithm ID= REQ_ID)	Yes	NA
REQ_MBIST_07	Supported(Algorithm ID= REQ_ID)	Yes	NA

5.6 Clocking

The Controller integrates a clock generation circuit to generate system reference clocks for the DDR PLL, the PCIe IO subsystem , and the whole chip's register blocks including CXL subsystem, microcontroller subsystem, and peripherals.

A stable external clock source is required, which is normally provided by the differential PCIe clock input on pins REFCLK0p/n. The Controller supports Spread Spectrum clocking on the clock source as defined by the PCI 5.0 Specification.

For the DDR PLL block, an external OSC clock (on pin EXT_CLK) can be used as a backup clock source, as selected by pin CLK_SEL. The DDR PLL is designed in the DDR subsystem to generate high-speed clocks for the DDR memory controller and DDR PHY in different applications with variable frequencies.

5.7 Resets

The Controller Full Chip Power on Reset (POR) is asserted after the device is powered on or once the external Full Chip Reset source is asserted.

This device provides three external Full Chip Reset sources on pins PERST0#, PERST1#, and PGOOD_CORE, which are selected by pins RESET_SEL[1:0] as shown in **Table 24**.

5.7 Resets (cont'd)

Table 24 — Reset Pins

RESET_SEL[1:0]	PERST0#	PERST1#	PGOOD_CORE	FULL CHIP RESET
00b	0	x	x	Asserted
	x	0	x	Asserted
	1	1	x	Norm Op
01b	X	x	0	Asserted
	x	x	1	Norm Op
10b	0	x	1	Asserted
	x	0	1	Asserted
	x	x	0	Asserted
	1	1	1	Norm Op
11b	RFU			

The pin PGOOD_DDR is used to indicate that the DDR power is ready. After the pin is asserted, the DDR controller subsystem reset exits.

5.8 SMBUS Subsystem

5.8.1 SMBus Responder Interface

The device supports one two-wire SMBus Responder interface for full access to the configuration registers in the device as well as an SMBus to I3C/I2C bridge to allow for reading of DIMM SPDs, temperature sensor, etc.

5.8.1.1 SMBus Responder Address

As referenced in CXL Device Management Specification the controller uses 3Ah as the SMBus responder address.

5.8.1.2 SMBus Command Formats

The SMBus interface responds to the SMBus commands. Refer to the SMBus specification for the detailed description of these commands.

Table 25 — SMBus System Requirements

Requirement ID	Baseline	Configurable	Default
REQ_SMBUS_Sys	Supported	Yes	NA

5.8.2 I3C Initiator Interface

The controller shall support I3C basic V1.1.1 support. The controller shall be able to support I3C initiator and I3C subordinate use case. The controller also shall be able to operate in I2C mode, the mode selection is configured via firmware.

Note, the controller design must ensure its I3C interface does not sample the CLK and data at the same time it is driving.

The I3C Initiator provides a two-wire interface based on SDA and SCL to connect with the external DDR memory system RDIMM/UDIMM SPDs or other Responder devices on the same I3C bus. I3C is backward compatible with Legacy I2C Devices. The I3C Bus Interface must co-exist with other devices using the same bus on the DIMM, including Temperature Sensor, SPDs, and PMIC devices.

5.9 On-Die RAM

The Controller may be implemented with some capacity of on-die RAM – for use as buffers, or for microcontroller code/storage, or other purposes. Any on-die RAM shall be implemented with:

1. Error Detection/Correction:
 - a. Embedded DRAM – SECDED level detection/correction across a codeword no larger than 64b
 - b. SRAM – Parity across a maximum of 16b
2. Reporting:
 - a. Correctable errors shall be reported via Informational event logs.
 - b. Uncorrectable and Parity Errors shall be reported via the Warning, Error, or Fatal event logs as appropriate.
 - c. Uncorrectable and Parity Errors that impact the device payload data integrity shall result in :
 - i. Poison status of any read data returned to the host.
 - ii. Blocking of any writes to the DRAM media

5.10 Microcontroller Subsystem

The Controller supports the use of one or more on-board microcontrollers. The specific choice of Microcontroller and ISA is left to the individual implementation.

The microcontroller can be set to boot from multiple sources, and it has direct access to the full on-board memory and PCIe address space.

The microcontroller shall be implemented such that firmware updates and activations do not disrupt the DRAM to System data path.

5.10.1 Booting

The Controller shall implement a secure boot protocol as defined in CXL Memory Device Management Reference Specification JESD-325.

5.10.2 Interrupt Controller

The Interrupt controller handles interrupt requests from multiple sources within the Controller and generates an IRQ Vector for the Microcontroller core. The interrupt handler must support:

1. Support a minimum of 8 interrupt requests.
2. Support separated enable register for each interrupt request.
3. Reading of the interrupt status.
4. Clearing of interrupt status via a register write.

Table 26 — Interrupt Vector Example

Vector Number	Component	IRQ Handler Address	Description
0	timer0	Boot Address + 0x00	
1	...	Boot Address + 0x04	
etc.	

5.10.3 Programmable Timers

The Controller should include one more configurable time interval counters. If an interrupt mode is enabled, a counter increases from zero to a configurable maximum value. The timer can trigger interrupt requests to the Microcontroller(s) upon after count expiration. The counters support three modes, selected by a register configuration:

1. Single mode: Counter swap to zero after reaching the max value and then the timer is disabled.
2. Multi-mode: Counter resets to zero after reaching the max value and continues to increment. Timer is always enabled in this mode by default.
3. Start-Stop mode: The start, stop, and reset of the timer is controlled via a programmable register. This mode is useful for time interval measurements.

5.10.4 Watchdog Timer(s)

If the Controller includes a microcontroller implementation, a minimum of at least one watchdog timer shall be implemented. The watchdog timer is used to safeguard against Microcontroller lockup. It shall have the following features:

1. Combinations of interrupt and reset when the watchdog timer expires.
2. Write protection mechanism for the Control/Reset Registers.
3. Configurable magic numbers for reset/restart of the timer.

5.10.4 Watchdog Timer(s) (cont'd)

The watchdog timer provides two-stages of mitigation in the event of a lockup:

1. Interrupt: If the Watchdog is not reset within a time not to exceed preset feature parameter, an Interrupt shall be issued to the associated Microcontroller.
2. Reset: If the Watchdog is not reset within an additional time not to exceed preset feature parameter, a reset shall be issued to the associated Microcontroller.

5.11 SPI Subsystem and Firmware

The SPI subsystem controls access to the external SPI flash memory. It includes support for:

1. Standard (single I/O) mode
2. Dual I/O mode
3. Quad I/O mode

To maximize the supported media types, the controller supports four different SPI data sample modes - allowing for different configurations of SPI clock's phase and polarity.

Data transfer capabilities include:

1. 1~32bit serial data transfer based on TX/RX FIFO architecture.
2. Big- and Little-Endian support
3. Data packaging
4. Configurable RX/TX operation based on interrupt or polling mechanism.
5. Programmable SPI IO[3:0] direction mapping
6. Programmable SPI data line status

5.11.1 Firmware Update

The Controller shall implement firmware update functionality as defined in CXL Memory Device Management Reference Specification JESD-325.

5.12 Error Reporting and Handling

The section Memory controller RAS and ECC describes the RAS feature requirements for the CXL memory controller device. This section describes the handling and reporting for detected errors through the previously described feature(s) and/or controller implementation specific. The requirement to support the reporting as described below, is conditional on controller's ability to detect the error condition.

The CXL memory controller shall support following configurable knobs as defined in the **Controller Configuration** section:

5.12 Error Reporting and Handling (cont'd)

Table 27 — Error Handling Knobs

Configuration knob	Default	Expected behavior
signal_viral_for_fatal_error	0	The controller shall signal Viral bit (and viral condition) if fatal error is detected
Write_pscub_corr_data	1	The controller shall write the data corrected during the patrol scrub operation back to the memory
Write_poison_for_unocrr	1	For read transaction if uncorrectable data is read , the controller shall write poison bit to the memory. The controller shall corrupt the write data intentionally to ensure UECC error and poison for subsequent read to the same address
Demand_scrub	1	Write the corrected ECC data to the memory

There are two thresholding mechanisms provided in the CXL specification for correctable errors:

1. Corrected Volatile Memory Error Programmable Warning values in Set Alert Configuration (section 8.2.9.9.3.3). While using this method, the controller reports the event when the threshold is reached (referred to as CVME threshold in table below) as DRAM event with event descriptor[0] = 0 (to indicate correctable event) and appropriate telemetry covered in the event type, subtype etc.
2. Advanced Error Threshold configuration as configured in Advanced Programmable CVME Threshold Feature(referred to as Advanced CVME Threshold in table below) . While using this method, the controller shall report event with event descriptor [1]=1 along with appropriate values in Advanced Programmable Corrected Memory Error Threshold Event Flags and CVME Count at Event. The controller shall support the capability to program leaky counters.

The controller shall support both methods of threshold configuration. The controller shall be able to support threshold values up to a minimum of 1.

Table 28 describes event and reporting actions. Please note, the threshold event referred to in the table refers to Advanced CVME Threshold events.

5.12 Error Reporting and Handling (cont'd)

Table 28 — Error Handling Requirements

Event	Event detected as / manifests as	Severity for the reported event	Event Reporting (Event Record/register) via CXL Interface	Device Handling (if applicable)	Additional flags	Comment
RwD with poison=1	Host uncorrectable ECC in write data source and writes poison to CXL memory	NA	None	Store the poison information per cache line		
REQ to address previously written with poison=1	Read (host read/patrol scrub read) to address previously written with poison=1	NA	None	DRS with poison=1		
Uncorrectable cache tag / metadata	Uncorrectable ECC reading tag during REQ or RwD	Failure	CXL protocol error (Uncorrectable Error Status Register.Internal_Error)	May send Viral to the host		
Firmware initialization failure	Firmware boot failure/timeout	Failure	Memory Device Status Register.FW Halt, and Memory Device Status Register.Device Fatal (8.2.8.5.1)			Depending on device implementation may result in fatal error/Viral
DRAM initialization failure	DRAM POST failure	Failure	Memory Device Status Register.Media Status (8.2.8.5.1), ; Also, in DRAM Event Record			
Controller initialization failure	Controller POST failure	Failure	None	None		CXL link will not come up
Runtime firmware assert	Management firmware assert at runtime	Failure	Memory Device Status Register.FW Halt (8.2.8.5.1)	Send Viral to the host		
Unrecoverable Internal Sideband Bus Protocol Error (e.g., SPD)	Discovery	Failure	Report sideband buserror in MMER(8.2.9.2.1.3)			
Invalid SPD Data on Sub-FRU	Discovery	Warning	Report MMER(8.2.9.2.1.3). Device Event Type			

Event	Event detected as / manifests as	Severity for the reported event	Event Reporting (Event Record/register) via CXL Interface	Device Handling (if applicable)	Additional flags	Comment
			= Memory Media FRU Error Subtype= Invalid Configuration Data			
Unsupported SPD Data on Sub-FRU	Discovery	Warning	Report MMER(8.2.9.2.1.3). Device Event Type = Memory Media FRU Error Subtype= Unsupported Configuration Data			
Invalid Sub-FRU Population	Discovery	Warning	Report MMER(8.2.9.2.1.3). Device Event Type = Memory Media FRU Error Subtype= Unsupported Media FRU			
PMIC – Fault on Previous Power On	Discovery	Failure	Report MMER(8.2.9.2.1.3). Device Event Type = Power Management Fault Component Identifier -> PMIC	Write to clear		
PMIC – Fault during Startup	PMIC Startup	Failure	Report MMER(8.2.9.2.1.3). Device Event Type = Power Management Fault Component Identifier -> PMIC	Sticky through next power cycle	HW replacement needed	
Correctable CA Parity (Retry)	Run Time: Each event of CA parity error detection	None	none	Retry the transactions up to programmed threshold value		
Correctable CA Parity	Run time: Number of CA parity errors > CVME Threshold	Warning	Internal Data Path Error in DRAM Event record		Maintenance needed	
Threshold CA Parity	Run time: Number of CA parity errors > Advanced CVME Threshold	As programmed	DRAM Event Record Memory Event Descriptor= Threshold Event		Maintenance needed	Leaky bucket to be programmed

Event	Event detected as / manifests as	Severity for the reported event	Event Reporting (Event Record/register) via CXL Interface	Device Handling (if applicable)	Additional flags	Comment
			.Memory Event= 05h, with appropriate DPA, Transaction type, telemetry			
Uncorrectable CA Parity	Number of retries for CA parity have exceeded the pre-configured controller retry_count_threshold	Failure	Report Uncorrectable Event. Internal Data Path Error in DRAM Event record	Vital if single channel*; read transaction receives poison=1 in DRS	Maintenance needed	
Small Eye, Poor Margins	Small Eye, Poor Margins as determined by the vendor criterion	Failure	Report Uncorrectable event, media initialization error DRAM Event Record.Memory Event= Data Path Error; Event Sub-Type= Medial Link Command Training Error. and Memory Device Status Register.Media Status			Criterion vendor dependent
Media testing (MBIST) Correctable errors	errors during host/controller-initiated testing	Warning	Report correctable event, media initialization error DRAM Event Record.Memory Event= Data Path Error; Event Sub-Type= Medial Link Command Training Error		None	
Media testing (MBIST) Uncorrectable errors	Media testing (MBIST) Uncorrectable errors (host/controller-initiated testing)	Failure	Report Uncorrectable event, media initialization error DRAM Event Record.Memory Event= Data Path Error; Event Sub-Type= Medial Link Command Training Error		HW replacement needed	
Correctable Data (ECC) Error	Correctable Data (ECC) Error (single	No	no	If demand scrub is enabled, write corrected data in the memory	None	

Event	Event detected as / manifests as	Severity for the reported event	Event Reporting (Event Record/register) via CXL Interface	Device Handling (if applicable)	Additional flags	Comment
	error i.e., < threshold)					
Correctable Data (ECC) Error	Correctable Data (ECC) Error > CVME Threshold	Warning	Report correctable event in DRAM event record, with appropriate DPA, Transaction type, telemetry, correction/nibble mask	If demand scrub is enabled, write corrected data in the memory	None	Use leaky bucket functionality
Threshold Correctable Data (ECC) Error	Correctable Data (ECC) Error > Adv CVME Threshold	As programmed	DRAM Event Record Memory Event Descriptor= Threshold Event .Memory Event= 05h, with appropriate DPA, Transaction type, telemetry	If demand scrub is enabled, write corrected data in the memory	None	Use leaky bucket functionality
Uncorrectable Data ECC error	Uncorrectable Data ECC error	Failure	Report uncorrectable event in DRAM event record, with appropriate DPA, Transaction type, telemetry	For read transaction , report poison bit in DRS. Based on configurable bit- write the poison bit and corrupt data to memory. Add to poison list if supported.	None	
Correctable Data (ECC) Error on patrol scrub(single < Threshold)	Correctable Data (ECC) Error on patrol scrub	None	none	Based on configurable bit write_pscrub_cor_r_data is enabled, write corrected data in the memory	None	
Correctable Data (ECC) Error on patrol scrub	Correctable Data (ECC) Error on patrol scrub > CVME Threshold	Warning	Report correctable event in DRAM event record, with appropriate DPA, Transaction type, telemetry, correction/nibble mask	Based on configurable bit write_pscrub_cor_r_data is enabled, write corrected data in the memory	None	
Threshold Correctable Data (ECC)	Correctable Data (ECC) Error on patrol	As Programmed	DRAM Event Record	Based on configurable bit write_pscrub_	None	

Event	Event detected as / manifests as	Severity for the reported event	Event Reporting (Event Record/register) via CXL Interface	Device Handling (if applicable)	Additional flags	Comment
Error on patrol scrub	scrub > Adv CVME Threshold		Memory Event Descriptor= Threshold Event .Memory Event= 05h, with appropriate DPA, Transaction type, telemetry	corr_data is enabled, write corrected data in the memory		
Uncorrectable Data ECC error on patrol scrub	Uncorrectable Data ECC error on patrol scrub	Failure	Report uncorrectable event in DRAM event record, with appropriate DPA, Transaction type, telemetry	Write poison bit and corrupt data to the memory location. Add to poison list if supported.	None	
ECS error	DRAM device ECS error reporting	Warning	Populate error information in DDR5 ECS log(8.2.9.5.2.4)		None	
Correctable Write CRC (Retry)	Run Time: Each event of WR CRC error detection	None	none	Retry the transactions up to programmed threshold value	None	
Correctable Write CRC	Run time: Number of WR CRC errors > Threshold programed in Adv Thresh event	warning	Report threshold event in DRAM event record, DRAM Event Record.Memory Event= Data Path Error; Event Sub-Type= Media Link CRC error		Maintenance needed	
Correctable Write CRC (Adv Threshold)	Run time: Number of WR CRC errors > Threshold programed in Adv Thresh event	As programmed	DRAM Event Record Memory Event Descriptor= Threshold Event .Memory Event= 05h, with appropriate DPA, Transaction type, telemetry		Maintenance needed	
Uncorrectable Write CRC	Number of retries for WR CRC have exceeded the pre-configured controller retry_count_threshold	Failure	Report uncorrectable event in DRAM event record, DRAM Event Record.Memory Event= Data Path Error; Event Sub-	Retry the transactions up to programmed threshold value	None	

Event	Event detected as / manifests as	Severity for the reported event	Event Reporting (Event Record/register) via CXL Interface	Device Handling (if applicable)	Additional flags	Comment
			Type= Media Link CRC error			
Correctable Read CRC (Retry)	Run Time: Each event of RD CRC error detection	None	none	Retry the transactions up to programmed threshold value	None	
Correctable Read CRC	Run time: Number of RD CRC errors > Threshold programed in Adv Thresh event	warning	Report threshold event in DRAM event record, DRAM Event Record.Memory Event= Data Path Error; Event Sub-Type= Media Link CRC error			
Correctable Read CRC (Adv Threshold)	Run time: Number of RD CRC errors > Threshold programed in Adv Thresh event	As programmed	DRAM Event Record Memory Event Descriptor= Threshold Event .Memory Event= 05h, with appropriate DPA, Transaction type, telemetry		None	Use leaky bucket functionality
Uncorrectable Read CRC	Number of retries for RD CRC have exceeded the pre-configured controller retry_count_threshold	Failure	Report uncorrectable event in DRAM event record, with Record.Memory Event= Data Path Error; Event Sub-Type= Media Link CRC error	Retry the transactions up to programmed threshold value. Report poison to the host. Update poison list if supported	None	
Row Hammer Issues	RFM failures	Warning	Report DRAM Event log, internal data path error		Maintenance needed	
CXL Link CRC Error(Threshold)	Link CRC detected by Device	Warning	Record threshold event CRC_Threshold_hit in correctable Error Status Register (8.2.4.16.4)	Retry the FLITS, Recovery after threshold	None	

Event	Event detected as / manifests as	Severity for the reported event	Event Reporting (Event Record/register) via CXL Interface	Device Handling (if applicable)	Additional flags	Comment
CXL Link Down	Link changes from L0 to LTSSM.Detect for > 256 ms or PERST#	Warning	Error isolation triggered at the host	None	None	
Partial Media training	Not all of the media behind the device trained successfully	Warning	Capacity reduction needed	None	Maintenance needed	
PMIC – Fault during runtime	PMIC runtime error	Failure	Report PM Fault bus error in MMER(8.2.9.2.1.3),	signal Viral Sticky through next power cycle	HW replacement needed	
CXL Link interface degraded to x2 or x1	CXL link training /run-time failure	Warning			Maintenance needed and Performance degraded	
Uncorrectable Internal RAM error(transaction address/opcode distinguishable)	Uncorrectable Structure parity/ ECC error on any internal RAM	Failure	Report uncorrectable event in DRAM event record, with appropriate transaction type, memory event type /subtype to indicate internal data path error	Poison data response if read transaction		
Uncorrectable Internal RAM error(transaction address/opcode NOT distinguishable)	Uncorrectable Structure parity/ ECC error on any internal RAM	Failure		Report Viral	NA	NA
Poison injection	Poison injection via mailbox commands	None	None	None		

5.12.1 Performance monitoring

The CXL Memory controller shall support CXL Performance Monitoring Unit instance(s) as referred to in CXL specification v3.0 section 13.2. It is recommended that CMC support a CPMU instance per memory controller channel, and one CPMU for each CXL Interface block. The CMC shall support at least one CPMU instance for entire CMC. Each CPMU shall be capable of supporting at least 8 configurable counters and may optionally support one fixed counter with clock ticks as event. The counters shall support capability to filter as supported in the event group definition.

The CMPU shall support the events described in the CXL vendor id group in table 13-5 of CXL 3.0 Specification and Event group DDR (Event Group = 8000h). The CPMU also shall support all events for supported opcodes in the Event Group for CXL.mem (Event group 20h, 21h, 24h, 25h). The event group 22h, 23h are not required in this version of specification.

The diagram in **Figure 9** shows a reference for CPMU instance per memory controller channel.

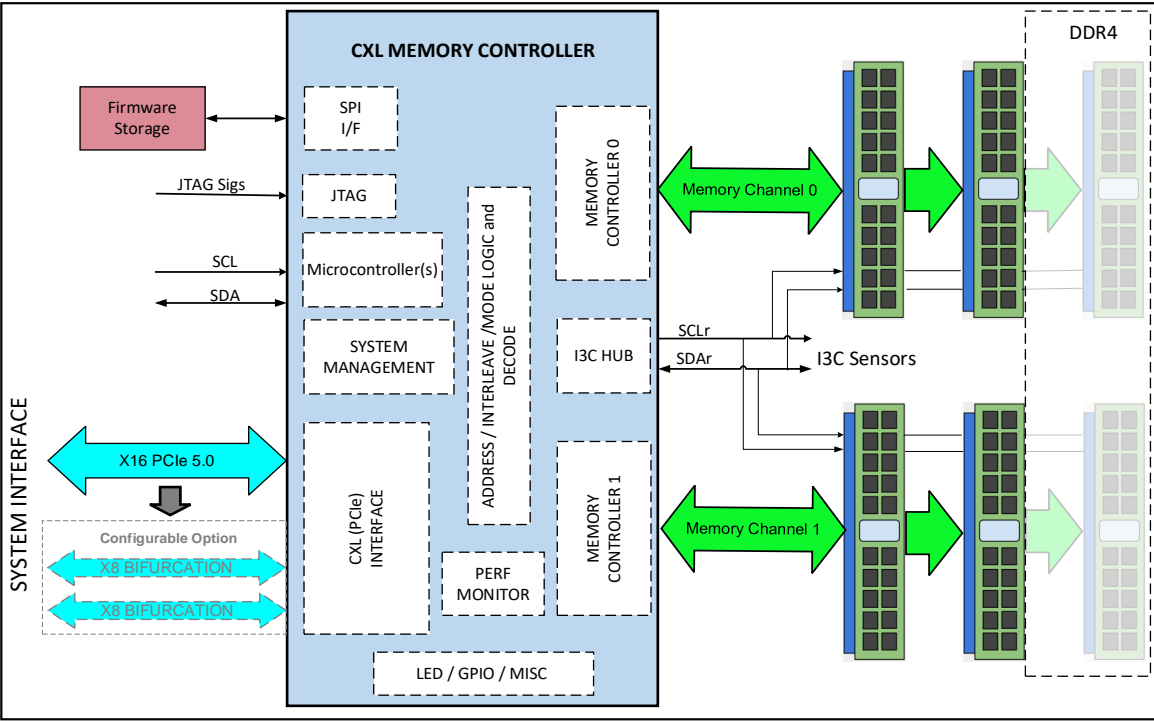


Figure 9 — Example Block Diagram for CXL Memory Controller

Table 29 indicates performance monitoring unit requirements and optionality as *_CPMU_*.

Table 29 — Performance Monitoring Requirements

Requirement ID	Baseline	Configurable	Default
REQ_CPMU_CXL	Supported	Yes	NA
REQ_CPMU_MC	Supported	Yes	NA

6 Performance Requirements

6.1 CXL Bandwidth

The following CXL bandwidth specifications are intended to provide throughput targets to Controller implementors. These specs are not to be considered throttled by media characteristics and assume a PCIe link at Gen5 speeds and minimal feature set as defined in the specification here enabled.

The CXL memory controller shall support following utilization and throughput targets for native CXL link widths (including bifurcation modes)

- 100% Stream Reads
 - $\geq 80\%$ efficiency of raw memory bandwidth
 - ≥ 51 GB/s or greater throughput for x16 and 25 GB/s or greater for x8 (potentially limited by CXL Link BW, example value corresponds to DDR5-4800)
- 100% Stream Writes
 - $\geq 75\%$ efficiency of raw memory bandwidth
 - ≥ 48 GB/s or greater throughput for x16 and 21 GB/s or greater for x8 (potentially limited by CXL Link BW, example value corresponds to DDR5-4800)
- For 2R1W random traffic
 - $\geq 70\%$ efficiency of raw memory bandwidth

Note that memory allocation mode and other settings may have an impact on the bandwidth balance between ports.

6.2 Controller Latency

Latency shall be measured from receiving a command flit at the PCIe PHY to sending the data response / completion flit on the PCIe PHY while operating at Gen 5 PCIe speeds. Latency shall not include external components such as DRAM, PCB trace, RCD's etc., but instead is intended to capture the controller component of the round-trip latency (as depicted in **Figure 10**). The latency targets are indicated as average latency with minimal required features enabled and any performance optimization features that CXL memory controller may have added as well.

The latency requirements are specified in terms of multiple performance bins. The CMC shall publish the expected performance bin in the host configuration/status interface as defined in the **Controller Configuration**. The latency requirements are specified in terms of no-greater-than the noted value for a given performance bin and controller shall publish the lowest, i.e., best bin possible. The controller shall publish the latency measurement at highest supported DDR speed bin – for example DDR4-3200 and DDR5-6400.

6.2 Controller Latency (cont'd)

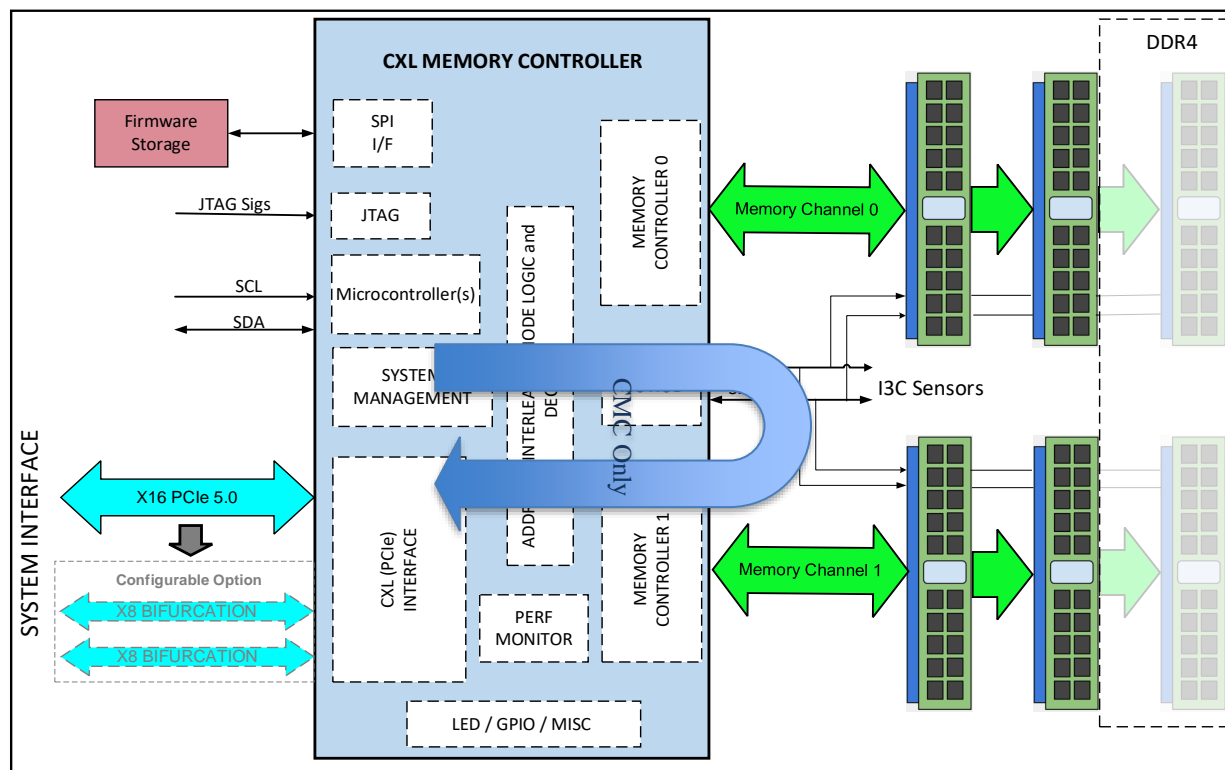


Figure 10 — Latency Path

6.2.1 Latency Requirements

The CXL Memory Controller device idle latency is characterized as nearly un-loaded latency for a read transaction.

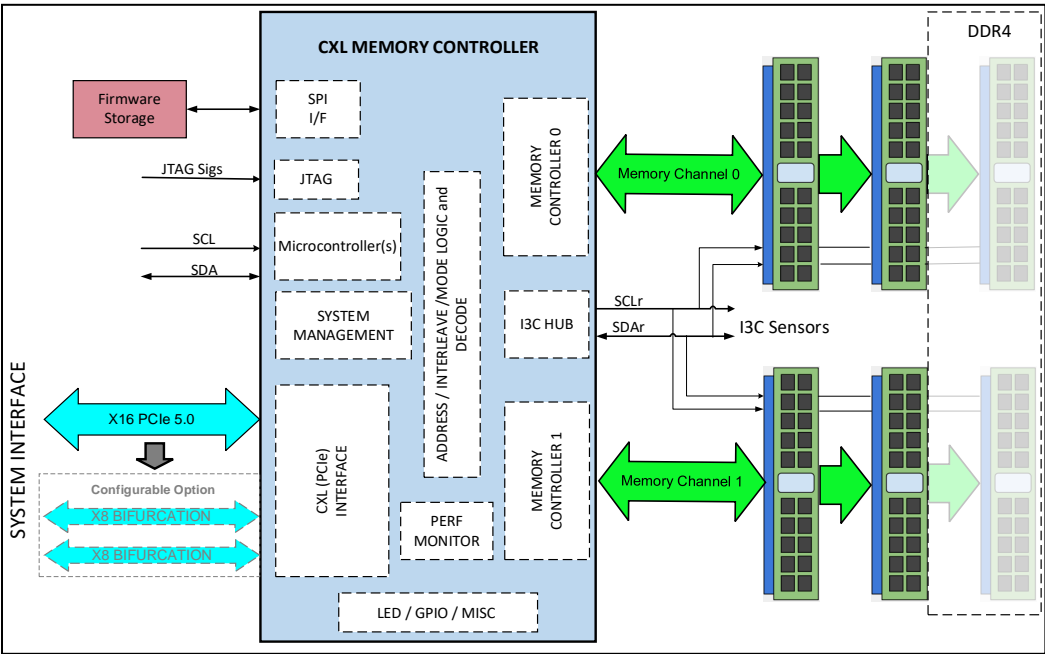
The loaded latency can be characterized as latency measurement at 60% utilization point of raw memory bandwidth with 2Rank or equivalent memory population, with 2R1W traffic mix with RANDOM addressing being generated by application. It may be noted that 2R1W is rough distribution of read and write transaction as received at CMC input over sample window time. The sample window shall include at least 10000 transactions.

Table 30 — CMC Performance Bins

Performance Bins	Unloaded Latency (No Greater than) (ns)	Loaded Latency (No Greater than at Specified Point) (ns)
40-100	40	100
45-120	45	120
50-125	50	130
60-150	60	150
70-200	70	200

6.2.1 Latency Requirements (cont'd)

Implementation Note: The latency measured may vary based on the performance optimization knobs and topology. For example, using common clock on PCIe/CXL interface, enabling sync header bypass, drift buffer optimization may yield better latency. In addition to these, the controller may have march specific features to enable bypass paths and/or scheduling algorithm options to present best possible latency behavior. The controller may enable these features in addition to the base required features called throughout this specification for performance measurement.



As depicted in the **Figure 10 — Latency Path**, the overall latency through the CXL memory device is aggregate latency through CXL Memory controller(CXL Phy + CXL Interface + Memory Controller + DDR Phy), DRAM channels, DRAM media.

Table 31 illustrates media access latency variation across different scenarios. The example considered here is DDR5-5600AN.

Table 31 — Example Latency

Scenario	Sequence	Parameters	Latency in ns
Page Miss Different bank	Activate -> CAS -> Data	tRCD+tAA	= 2*14.285 = 28.57 ns
Page Miss Same Bank	Precharge -> Activate -> CAS -> Data	tRP + tRCD+tAA	= 3*14.285 = 42.885
Page Hit	CAS-> Data	tRCD	= 14.285

The latency reported in performance bin is indicative of CMC latency only and excludes the media, channel latency.

Table 32 — Latency Bin Requirement

Requirement ID	Baseline	Configurable	Default
REQ_LATENCY_BIN	Supported	No	NA

7 Power and Thermal

7.1 Power Requirements

7.1.1 Absolute Maximum

Under no conditions with operational limits shall the controller power requirements exceed 14 W for x16 controller and 11 W for x8 controller.

The table below indicates absolute maximum power requirements as *_IF_*_MAX_POWER.

Table 33 — Power Requirement

Requirement ID	CXL Config	Power (W)
REQ_IF_X8_MAX_POWER	X8 Gen 5	11 W or less
REQ_IF_X16_MAX_POWER	X16 Gen 5	14 W or less

7.1.2 Normal Operation Limits

The specification describes power requirement at specified operating conditions. The power for CMC is recommended to be within the limits defined in **Table 34** when measured at the following conditions:

1. 75 °C Tj or less, typical process, and nominal supply voltages
2. Mixed random read/write workload – 67% reads, 33% writes.
3. 10% page hit rate.
4. Minimal feature set as described in the specification enabled.
5. Sustained measurement over 100 µs window.

Table 34 — Power Measured for Various Configurations

CXL Config	Memory Config	Power (W)
X8 Gen 5 – Option 2	1 x 72b DDR4 - 3200	6 W or less
X8 Gen 5 – Option 2	1 x 80b DDR5 - 6400	7 W or less
X16 Gen 5 - Option 1	2 x 72b DDR4 - 3200	8 W or less
X16 Gen 5 – Option 1	2 x 80b DDR5 - 6400	10 W or less

7.1.2 Normal Operation Limits

Implementation note:

It may be noted that the measured power may vary depending on various operating conditions and configurations. For example, feature such as CXL link encryption IDE, may add to power measured. For controller implementations supporting additional features such as compression (out of the scope for the current specification), it is advised to disable the features for power characterization while measuring against the above specified limits. The power may also vary with the DRAM speed of operation.

7.2 Thermal Requirements

7.2.1 On-die Thermal Sensor

The Controller shall implement an on-die thermal sensor. Additionally, the thermal sensor topology, sensor requirements and system interface are covered in CXL Device Management specification section 8.

C. CONFIGURATION INTERFACE

8 Controller Configuration

8.1 Overview

Specification of the JEDEC Memory Controller Specification for Compute Express Link (CXL) configuration is defined in several documents. The three principal documents are the PCIe 5.0 specification, the CXL 3.1 specification, the CXL Memory Device Management Reference Standard and this document, JESD319 JEDEC Memory Controller Specification for Compute Express Link (CXL). This section specifies controller configuration not covered by the PCIe 5.0 and CXL 3.1 specifications.

8.2 Get Feature and Set Feature

Get Feature and Set Feature are used for features and functionality that require host visibility and/or control in a consistent manner. These CCI Opcodes are defined in CXL Specification 3.0, version 1.0 Table 8-36. This section defines the features that may be read or written using Get Feature and Set Feature. The features are UUID based.

8.2.1 Supported Feature Entry Structure

The host queries the controller with the Get Supported Feature (see section 8.2.9.6.1. of CXL 3.1). The controller responds with a list of supported features with each supported feature containing an entry following the structure described in CXL 3.1 Table 8-97 Get Supported Features Supported Feature Entry.

8.2.2 Controller Configuration Get Supported Feature Entries

Values for the entries returned for the Get Supported Features command code.

Table 35 — Supported Feature Entries

Attribute	Addressing Policy	RAS Features	CMC Refresh	Dual Port
Feature Identifier	f182ccf8-72bd-11ee-b962-0242ac120002	5174e599-1430-433e-af4b-5772bae6cc91	b44897af-bddb-4e9b-9d74-dbab49062f7b	b00726e4-de86-4205-b27f-b0bb6825660d
Feature Index	Device Specific	Device Specific	Device Specific	Device Specific
Get Feature Size	02h	13h	02h	21h
Set Feature Size	02h	0Ch	02h	21h
Attribute Flags	Bit[0]: 1 - Feature attributes can be changed Bits[3:1]: 100b - Cold reset. Bit[4]: 0 – Does not persist across firmware update Bit[5]: 1 - Default selection value Bit[6]: 1 - Saved selection supported Bits[31:7]: Reserved	Bit[0]: 1 - Feature attributes can be changed Bits[3:1]: 100b - Cold reset. Bit[4]: 0 – Does not persist across firmware update Bit[5]: 1 - Default selection value Bit[6]: 1 - Saved selection supported Bits[31:7]: Reserved	Bit[0]: 1 - Feature attributes can be changed Bits[3:1]: 100b - Cold reset. Bit[4]: 0 – Does not persist across firmware update Bit[5]: 1 - Default selection value Bit[6]: 1 - Saved selection supported Bits[31:7]: Reserved	Bit[0]: 1 - Feature attributes can be changed Bits[3:1]: 100b - Cold reset. Bit[4]: 0 – Does not persist across firmware update Bit[5]: 1 - Default selection value Bit[6]: 1 - Saved selection supported Bits[31:7]: Reserved
Get Feature Version	0	0	0	0
Set Feature Version	0	0	0	0

Attribute	Addressing Policy	RAS Features	CMC Refresh	Dual Port
Set Feature Effects (SFE)	Bit[0]: 1 (Configuration Change after Cold Reset) Bit[1]: 0 (Immediate Configuration Change) Bit[2]: 0 (Immediate Data Change) Bit[3]: 0 (Immediate Policy Change) Bit[4]: Vendor-specific value (Immediate Log Change) Bit[5]: 0 (Security State Change) Bit[6]: 0 (Background Operation) Bit[7]: Vendor-specific value (Secondary Mailbox Supported) Bit[8]: 0 (Request Abort Background Operation Supported) Bit[9]: 1 (SFE[11:10] Valid) Bit[10]: 0 (Configuration Change after Conventional Reset) Bit[11]: 0 (Configuration Change after CXL Reset)	Bit[0]: 1 (Configuration Change after Cold Reset) Bit[1]: 0 (Immediate Configuration Change) Bit[2]: 0 (Immediate Data Change) Bit[3]: 0 (Immediate Policy Change) Bit[4]: Vendor-specific value (Immediate Log Change) Bit[5]: 0 (Security State Change) Bit[6]: 0 (Background Operation) Bit[7]: Vendor-specific value (Secondary Mailbox Supported) Bit[8]: 0 (Request Abort Background Operation Supported) Bit[9]: 1 (SFE[11:10] Valid) Bit[10]: 0 (Configuration Change after Conventional Reset) Bit[11]: 0 (Configuration Change after CXL Reset)	Bit[0]: 1 (Configuration Change after Cold Reset) Bit[1]: 0 (Immediate Configuration Change) Bit[2]: 0 (Immediate Data Change) Bit[3]: 0 (Immediate Policy Change) Bit[4]: Vendor-specific value (Immediate Log Change) Bit[5]: 0 (Security State Change) Bit[6]: 0 (Background Operation) Bit[7]: Vendor-specific value (Secondary Mailbox Supported) Bit[8]: 0 (Request Abort Background Operation Supported) Bit[9]: 1 (SFE[11:10] Valid) Bit[10]: 0 (Configuration Change after Conventional Reset) Bit[11]: 0 (Configuration Change after CXL Reset)	Bit[0]: 1 (Configuration Change after Cold Reset) Bit[1]: 0 (Immediate Configuration Change) Bit[2]: 0 (Immediate Data Change) Bit[3]: 0 (Immediate Policy Change) Bit[4]: Vendor-specific value (Immediate Log Change) Bit[5]: 0 (Security State Change) Bit[6]: 0 (Background Operation) Bit[7]: Vendor-specific value (Secondary Mailbox Supported) Bit[8]: 0 (Request Abort Background Operation Supported) Bit[9]: 1 (SFE[11:10] Valid) Bit[10]: 0 (Configuration Change after Conventional Reset) Bit[11]: 0 (Configuration Change after CXL Reset)

8.2.3 Addressing Policy

See the Supported Features entry for Addressing Policy in **Table 35 — Supported Feature Entries**.

Table 36 — Addressing Policy Feature Readable Attributes

Byte Offset	Length in Bytes	Description
00h	1h	Page Policy <ul style="list-style-type: none"> • 00h Open • 01h Closed • 02h Adaptive • 03h to FFh Vendor defined
01h	1h	Interleave Modes <ul style="list-style-type: none"> • 00h Linear • 01h Open Page • 02h Closed Page • 03h 3DS Open Page • 04h 3DS Closed Page • 05h to FFh Vendor defined config

Table 37 — Addressing Policy Feature Writeable Attributes

Byte Offset	Length in Bytes	Description
00h	1h	Page Policy <ul style="list-style-type: none"> • 00h Open • 01h Closed • 02h Adaptive • 03h to FFh Vendor defined
01h	1h	Interleave Modes <ul style="list-style-type: none"> • 00h Linear • 01h Open Page • 02h Closed Page • 03h 3DS Open Page • 04h 3DS Closed Page • 05h to FFh Vendor defined config

8.2.4 RAS Features

See the Supported Features entry for RAS Features in **Table 35 — Supported Feature Entries**.

Table 38 — RAS Features Readable Attributes

Byte Offset	Length in Bytes	Description
00h	1h	Informational Event Log Count <ul style="list-style-type: none"> 00h to FFh Informational event count of 0 to 255
01h	1h	Warning Event Log Count <ul style="list-style-type: none"> 00h to FFh Warning event count of 0 to 255
02h	1h	Failure Event Log Count <ul style="list-style-type: none"> 00h to FFh Warning event count of 0 to 255
03h	1h	Fatal Event Log Count <ul style="list-style-type: none"> 00h to FFh Fatal event count of 0 to 255
04h	1h	DRAM ECC <ul style="list-style-type: none"> 00h Single bit error detect and correct 01h Multi-bit error detect and correct 02h to FFh Vendor defined
05h	1h	Single Device Failure Correction Mode <ul style="list-style-type: none"> 00h Disabled 01h Enabled 02h to FFh Vendor defined config
06h	1h	Demand Scrubbing <ul style="list-style-type: none"> 00h Disabled 01h Enabled 01h to FFh reserved
07h	1h	Write CRC Supported <ul style="list-style-type: none"> 00h Not supported 01h Supported but disabled 02h Illegal 03h Supported and enabled 04h to FFh reserved
08h	1h	Write CRC Max Retries Configured <ul style="list-style-type: none"> 00h to FFh Retry Limit of 0 to 255

Byte Offset	Length in Bytes	Description
09h	1h	Write CRC Max Retries Supported <ul style="list-style-type: none"> 00h to FFh Retry Limit of 0 to 255
0Ah	1h	Read CRC <ul style="list-style-type: none"> 00h Not supported 01h Supported disabled 02h Illegal 03h Supported enabled 04h to FFh reserved
0Bh	1h	Read CRC Retries Configured <ul style="list-style-type: none"> 00h to FFh Retry Limit of 0 to 255
0Ch	1h	Read CRC Max Retries Supported <ul style="list-style-type: none"> 00h to FFh Retry Limit of 0 to 255
0Dh	1h	CA Parity Error Detection <ul style="list-style-type: none"> 00h Not supported 01h Supported disabled 02h Illegal 03h Supported enabled 04h to FFh reserved
0Eh	1h	CA Parity Consecutive Retries Configured <ul style="list-style-type: none"> 00h to FFh Retry Limit of 0 to 255
0Fh	1h	CA Parity Max Retries Supported <ul style="list-style-type: none"> 00h to FFh Retry Limit of 0 to 255
10h	1h	Signal_viral_for_fatal_error <ul style="list-style-type: none"> 00h Disabled 01h Enabled 01h to FFh reserved
11h	1h	Write_pscrub_corr_data <ul style="list-style-type: none"> 00h Disabled 01h Enabled 01h to FFh reserved
12h	1h	Write_poison_for_uncorr <ul style="list-style-type: none"> 00h Disabled 01h Enabled 01h to FFh reserved

8.2.4 RAS Features (cont'd)**Table 39 — RAS Features Writeable Attributes**

Byte Offset	Length in Bytes	Description
00h	1h	DRAM ECC <ul style="list-style-type: none"> • 00h Single bit error detect and correct • 01h Multi-bit error detect and correct 02h to FFh Vendor defined
01h	1h	Single Device Failure Correction Mode <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 02h to FFh Vendor defined config
02h	1h	Demand Scrubbing <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved
03h	1h	Write CRC <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved
04h	1h	Write CRC Retries <ul style="list-style-type: none"> • 00h to FFh Retry Limit of 0 to 255
05h	1h	Read CRC <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved
06h	1h	Read CRC Retries <ul style="list-style-type: none"> • 00h to FFh Retry Limit of 0 to 255
07h	1h	CA Parity Error Detection <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved
08h	1h	CA Parity Consecutive Retries <ul style="list-style-type: none"> • 00h to FFh Retry Limit of 0 to 255

Byte Offset	Length in Bytes	Description
09h	1h	Signal_viral_for_fatal_error <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved
0Ah	1h	Write_pscrub_corr_data <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved
0Bh	1h	Write_poison_for_uncorr <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved

8.2.5 Error Injection

8.2.6 CMC Refresh

See the Supported Features entry for CMC Refresh in **Table 35 — Supported Feature Entries**.

Table 40 — CMC Refresh Readable Attributes

Byte Offset	Length in Bytes	Description
00h	1h	DRFM (Directed Refresh Management) <ul style="list-style-type: none"> • 00h Not supported • 01h Supported disabled • 02h Illegal • 03h Supported enabled • 04h to FFh reserved
01h	1h	PRAC (Per Row Activation Counting) <ul style="list-style-type: none"> • 00h Disabled • 01h Enabled • 01h to FFh reserved
02h	1h	Additional Attributes Place holder for Additional attributes dependent on section Data Integrity Risk Mitigations

8.2.6 CMC Refresh (cont'd)

Table 41 — CMC Refresh Writeable Attributes

Byte Offset	Length in Bytes	Description
00h	1h	DRFM (Directed Refresh Management) Support <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved
01h	1h	PRAC (Per Row Activation Counting) <ul style="list-style-type: none"> • 00h Disable • 01h Enable • 01h to FFh reserved
02h	1h	Additional Attributes Place holder for Additional attributes dependent on section Data Integrity Risk Mitigations

8.2.7 SMBus

8.2.8 Microcontroller Subsystem

8.2.9 Bootstrap

Bootstrap configuration is used for features and functionality that must be defined when the controller is initialized and before host control is established.

8.2.10 Dual Port

When the CXL® interface is bifurcated through the DUALPORTEN_n the dual port configuration, described in the **Controller Configuration** defines the division of the attached memory capacity. This feature is only supported through CCI over MCTP so that the Host cannot modify the configuration. This feature may only be set on cold reset.

See the Supported Features entry for Dual Port in **Table 35 — Supported Feature Entries**.

8.2.10 Dual Port (cont'd)

Table 42 — Dual Port Readable Attributes

Byte Offset	Length in Bytes	Description
00h	1h	Dual Port <ul style="list-style-type: none"> • 00h Divided • 01h Sectioned • 01h to FFh reserved
01h	8h	Dual Port 0 Base Address <ul style="list-style-type: none"> • 00,000,000h to FF,FFF,FFF Address_Boundary of 0 to 18,446,744,073,709,551,615
09h	8h	Dual Port 0 Address Space Size 00,000,000h to FF,FFF,FFF Port size of 0 to 18,446,744,073,709,551,616 addresses
11h	8h	Dual Port 1 Base Address <ul style="list-style-type: none"> • 00,000,000h to FF,FFF,FFF Address_Boundary of 0 to 18,446,744,073,709,551,615
19h	8h	Dual Port 1 Address Space Size <ul style="list-style-type: none"> • 00,000,000h to FF,FFF,FFF Port size of 0 to 18,446,744,073,709,551,616 addresses

8.2.10 Dual Port (cont'd)**Table 43 — Dual Port Writeable Attributes**

Byte Offset	Length in Bytes	Description
00h	1h	Dual Port <ul style="list-style-type: none"> • 00h Divided • 01h Sectioned • 01h to FFh reserved
01h	8h	Dual Port 0 Base Address <ul style="list-style-type: none"> • 00,000,000h to FF,FFF,FFF Address_Boundary of 0 to 18,446,744,073,709,551,615
09h	8h	Dual Port 0 Address Space Size <ul style="list-style-type: none"> • 00,000,000h to FF,FFF,FFF Port size of 0 to 18,446,744,073,709,551,616 addresses
11h	8h	Dual Port 1 Base Address <ul style="list-style-type: none"> • 00,000,000h to FF,FFF,FFF Address_Boundary of 0 to 18,446,744,073,709,551,615
19h	8h	Dual Port 1 Address Space Size <ul style="list-style-type: none"> • 00,000,000h to FF,FFF,FFF Port size of 0 to 18,446,744,073,709,551,616 addresses

9 Implementation Note: Power and Signal Interfaces

Following clause describes the signal interfaces, pin out and packaging information for implementation reference. These are not normative requirements.

9.1 Power and Ground

This clause defines the power supply requirements for the Controller.

Table 44 — Power and Ground Signals

Name	Function	Voltage _{nom}
VDD_CORE	Core Power	0.75 V
VDD_DDR	DRAM I/O Power	1.1 V/1.2 V
V_SERDES	PCIe Serdes	1.2 V
V_ANALOG0	ANALOG DC Power	TBDV
V_ANALOG1	TBD Power	TBDV
V_MISC	GPIO, SPI, I3C, etc.	1.8 V
GND	Common ground return current	0V

9.2 Controller Interface Signal Groups

These clauses define the IO signals for the Controller, generally grouped by functionality, or subsection association.

9.2.1 X16 Controller Pin Interface and Definition

Please refer to additional specifications such as PCIe base specification, DDR4 DDR5 JEDEC specification, JEDEC I3C specification for additional details of operation.

The Controller must enable two DIMM-width memory channels and support DDR4 and DDR5 technology generations. Both channels shall be operated in either DDR4 or DDR5 compatible mode. Mixed mode operation is not supported. See JEDEC DDR4^[3] and DDR5^[4] specifications for details of operation.

9.2.1 X16 Controller Pin Interface and Definition (cont'd)

Table 45 — x16 CMC Pin Interface

IO Type	Interface	Pin	Description
O	DDR5	M0_SA_CKA_t, M0_SA_CKA_c, M0_SA_CKB_t, M0_SA_CKB_c, M1_SA_CKA_t, M1_SA_CKA_c, M1_SA_CKB_t, M1_SA_CKB_c	Sub-channel A Differential Output Clocks to DRAM/DIMMs. Clocks are grouped with sub-channel to facilitate single sub-channel operation in non-RCD systems.
O	DDR5	M0_SB_CKA_t, M0_SB_CKA_c, M0_SB_CKB_t, M0_SB_CKB_c, M1_SB_CKA_t, M1_SB_CKA_c, M1_SB_CKB_t, M1_SB_CKB_c	Sub-channel B Differential Output Clocks to DRAM/DIMMs. Clocks are grouped with sub-channel to facilitate single sub-channel operation in non-RCD systems.
O	DDR5	M0_SA_CS0_n, M0_SA_CS1_n, M0_SA_CS2_n, M0_SA_CS3_n, M1_SA_CS0_n, M1_SA_CS1_n, M1_SA_CS2_n, M1_SA_CS3_n	Sub-channel A Chip Select for each supported rank
O	DDR5	M0_SB_CS0_n, M0_SB_CS1_n, M0_SB_CS2_n, M0_SB_CS3_n, M1_SB_CS0_n, M1_SB_CS1_n, M1_SB_CS2_n, M1_SB_CS3_n	Sub-channel B Chip Select for each supported rank
O	DDR5	M0_SA_CA[6:0], M1_SA_CA[6:0]	Sub-channel A command/address bits[6:0] to DRAM (non-RCD systems) Sub-channel A command/ Address to RCD (RCD-based systems)
O	DDR5	M0_SA_CA7/M0_SA_DPAR, M1_SA_CA7/M1_SA_DPAR	Sub-channel A command/address bit[7] to DRAM (non-RCD systems) Sub-channel A command/address parity to RCD (RCD-based systems)
O	DDR5	M0_SA_CA[13:8], M1_SA_CA[13:8]	Sub-channel A command/address bits[13:8] to DRAM (non-RCD systems)
O	DDR5	M0_SB_CA[6:0], M1_SB_CA[6:0]	Sub-channel B command/address bits[6:0] to DRAM (non-RCD systems) Sub-channel B command/ Address to RCD (RCD-based systems)
O	DDR5	M0_SB_CA7/M0_SB_DPAR, M1_SB_CA7/M1_SB_DPAR	Sub-channel B command/address bit[7] to DRAM (non-RCD systems) Sub-channel B command/address parity to RCD (RCD-based systems)

IO Type	Interface	Pin	Description
O	DDR5	M0_SB_CA[13:8], M1_SB_CA[13:8]	Sub-channel B command/address bits[13:8] to DRAM (non-RCD systems)
I/O	DDR5	M0_SA_DQ[31:0], M1_SA_DQ[31:0]	Sub-channel A Data bits
I/O	DDR5	M0_SA_CB[7:0], M1_SA_CB[7:0]	Sub-channel A ECC/Check bits
I/O	DDR5	M0_SA_DQS{9:0}_t, M0_SA_DQS{9:0}_c, M1_SA_DQS{9:0}_t, M1_SA_DQS{9:0}_c	Sub-channel A Differential Data Strokes
I/O	DDR5	M0_SB_DQ[31:0], M1_SB_DQ[31:0]	Sub-channel B Data bits
I/O	DDR5	M0_SB_CB[7:0], M1_SB_CB[7:0]	Sub-channel B ECC/Check bits
I/O	DDR5	M0_SB_DQS{9:0}_t, M0_SB_DQS{9:0}_c, M1_SB_DQS{9:0}_t, M1_SB_DQS{9:0}_c	Sub-channel B Differential Data Strokes
I	DDR5	M0_ALERT_n, M1_ALERT_n	DRAM/DIMM parity error alert
O	DDR5	M0_RESET_n, M1_RESET_n	DRAM/DIMM asynchronous reset
A	DDR5	M0_ZQCAL, M1_ZQCAL	Reference pin for ZQ calibration of controller's DDR interface
I	DDR5	M0_DLBDQ, M1_DLBDQ	Loopback data from RCD.
I	DDR5	M0_DLBDQS, M1_DLBDQS	Loopback strobe from RCD.
O	DDR5	PWR_EN	UDIMM Only. Provides VR_EN for PMIC5100.
I/O	DDR5	PGOOD_DDR / PCAMP	PGOOD_DDR is UDIMM Only. Reports PWR_GOOD for PMIC5100.
O	DDR5	TEN	
O	DDR4	M0_CKA_t, M0_CKA_c, M0_CKB_t, M0_CKB_c, M1_CKA_t, M1_CKA_c, M1_CKB_t, M1_CKB_c	Differential output clocks to DRAM/DIMM.

IO Type	Interface	Pin	Description
O	DDR4	M0_CKC_t, M0_CKC_c, M0_CKD_t, M0_CKD_c, M1_CKC_t, M1_CKC_c, M1_CKD_t, M1_CKD_c	Differential output clocks to DRAM/DIMM
O	DDR4	M0_CS0_n, M0_CS1_n, M0_CS2_n, M0_CS3_n, M1_CS0_n, M1_CS1_n, M1_CS2_n, M1_CS3_n	Chip Select for each supported rank
O	DDR4	M0_CKE0, M0_CKE1, M0_CKE2, M0_CKE3, M1_CKE0, M1_CKE1, M1_CKE2, M1_CKE3	Clock Enable for each supported rank
O	DDR4	M0_ODT0, M0_ODT1, M0_ODT2, M0_ODT3, M1_ODT0, M1_ODT1, M1_ODT2, M1_ODT3	On-die Termination enable for each supported rank
O	DDR4	M0_ACT_n, M1_ACT_n	Activate command signal
O	DDR4	M0_A[17,13,11,9:0], M1_A[17,13,11,9:0]	Address pins, not including dual-purpose address/command pins.
O	DDR4	M0_RAS_n/M0_A16, M1_RAS_n/M1_A16	Dual purpose Row Address Strobe and A16
	DDR4	M0_CAS_n/M0_A15, M1_CAS_n/M1_A15	Dual purpose Column Address Strobe and A15
O	DDR4	M0_WE_n/M0_A14, M1_WE_n/M1_A14	Dual purpose Write Enable and A14
	DDR4	M0_BC_n/M0_A12, M1_BC_n/M1_A12	Dual purpose Burst Chop and A12
O	DDR4	M0_AP/M0_A10, M1_AP/M1_A10	Dual purpose Auto Precharge and A10
O	DDR4	M0_PAR, M1_PAR	Command/address parity input
O	DDR4	M0_BG[1:0], M1_BG[1:0]	Bank Group signals
O	DDR4	M0_BA[1:0], M1_BA[1:0]	Bank Address signals
O	DDR4	M0_CID[2:0], M1_CID[2:0]	Chip ID signals
I/O	DDR4	M0_DQ[63:0], M1_DQ[63:0]	Data bits
I/O	DDR4	M0_CB{7:0}, M1_CB{7:0}	ECC/Check bits

IO Type	Interface	Pin	Description
I/O	DDR4	M0_DQS{17:0}_t, M0_DQS{17:0}_c, M1_DQS{17:0}_t, M1_DQS{17:0}_c	Differential Data Strobcs
I	DDR4	M0_ALERT_n, M1_ALERT_n	DRAM/DIMM parity error alert
O	DDR4	M0_RESET_n, M1_RESET_n	DRAM/DIMM asynchronous reset
A	DDR4	M0_ZQCAL, M1_ZQCAL	Reference pin for ZQ calibration of controller's DDR interface
I	DDR4	M0_EVENT_n, M1_EVENT_n	Thermal event signal from DDR4 SPD Hub.
A	DDR4	M0_VrefCA, M1_VrefCA	
I	CXL	PECLK0_t, PECLK0_n, PECLK1_t, PECLK1_n	Differential PCIe Reference Clock
I	CXL	PERX{15:0}_p, PERX{15:0}_n	Differential PCIe Receiver signals
O	CXL	PETX{15:0}_p, PETX{15:0}_n	Differential PCIe Transmitter signals
I	CXL	PERST0_n, PERST1_n	PCIe Reset.
I	CXL	DUALPORTEN_n	Dual Port configuration enable
A	CXL	PERES0	Calibration Resistor pin.
I	I3C Host	HSCL	Host I2C/I3C Clock
I/O	I3C Host	HSDA	Host I2C/I3C Data
O	I3C Host	MSCL	Memory Card I2C/I3C Clock
I/O	I3C Host	MSDA	Memory Card I2C/I3C Data
I	UART	RXD	UART Receiver
O	UART	TXD	UART Transmitter
O	SPI	SCLK	SPI Clock signal
O	SPI	SCS_n	SPI Chip Select signal
I/O	SPI	SIO[3:0]	SPI Data
I	JTAG	TRST_n	TAP Controller asynchronous reset
I	JTAG	TCK	Test Clock

IO Type	Interface	Pin	Description
I	JTAG	TMS	Test Mode Select
I	JTAG	TDI	Test Scan Data In
O	JTAG	TDO	Test Scan Data Out
I	JTAG	TMUXSEL[1:0]	Select scan chain target: b00 - uController Debug b01 - PCIe Physical b1x - Reserved
I/O	GPIO	GPIO[7:0]	General Purpose IOs
O	GPIO	LED[2:0]	Status LEDs (Definition TBD)
I	Misc.	PWRDIS	Card 12V shutoff indicator in EDSFF spec
I	Misc.	PGOOD / RESET_n	Controller input power system stable / Release controller from reset
I	Misc.	REFCLK_p, REFCLK_n (Single Ended CLK Option: EXT_OSC_CLK)	Differential Controller input clock Option: Single Ended CLK Input
I	Misc.	CLKSEL [1:0]	PLL Reference Clock Source: 0 - PECLK0_p/n 1 - REFCLK_p/n
I	Misc.	RSTSEL[1:0]	Select primary reset source: b00 - PERST0_n & PERST1_n b01 - PGOOD (RESET_n) b10 - PGOOD (RESET_n) & PERST0_n & PERST1_n b11 - Reserved
I	Misc.	BOOTSEL[1:0]	Select internal CPU boot mode: b00 - Local ROM b01 - Local RAM b10 - Reserved b11 - External SPI
I	Misc.	RCVRY	RCVRY pin
I	Misc.	Vendor_Specific [9:8]	
I/O	Misc.	DEBUG[3:0]	Vendor specific debug pins

9.2.2 X8 Controller Pin Interface and Definition

Table 46 — x8 CMC Pin Interface

IO Type	Interface	Pin	Description
O	DDR5	MO_SA_CKA_t, MO_SA_CKA_c, MO_SA_CKB_t, MO_SA_CKB_c	Sub-channel A Differential Output Clocks to DRAM/DIMMs. Clocks are grouped with sub-channel to facilitate single sub-channel operation in non-RCD systems.
O	DDR5	MO_SB_CKA_t, MO_SB_CKA_c, MO_SB_CKB_t, MO_SB_CKB_c	Sub-channel B Differential Output Clocks to DRAM/DIMMs. Clocks are grouped with sub-channel to facilitate single sub-channel operation in non-RCD systems.
O	DDR5	MO_SA_CKC_t, MO_SA_CKC_c, MO_SA_CKD_t, MO_SA_CKD_c	Additional copies of Sub-Channel A Differential Output Clocks to DRAM/DIMMs
O	DDR5	MO_SB_CKC_t, MO_SB_CKC_c, MO_SB_CKD_t, MO_SB_CKD_c	Additional copies of Sub-Channel B Differential Output Clocks to DRAM/DIMMs
O	DDR5	MO_SA_CS0_n, MO_SA_CS1_n, MO_SA_CS2_n, MO_SA_CS3_n	Sub-channel A Chip Select for each supported rank
O	DDR5	MO_SB_CS0_n, MO_SB_CS1_n, MO_SB_CS2_n, MO_SB_CS3_n	Sub-channel B Chip Select for each supported rank
O	DDR5		
O	DDR5	MO_SA_CA[6:0]	Sub-channel A command/address bits[6:0] to DRAM (non-RCD systems) Sub-channel A command/ Address to RCD (RCD-based systems)
O	DDR5	MO_SA_CA7/MO_SA_DPAR	Sub-channel A command/address bit[7] to DRAM (non-RCD systems) Sub-channel A command/address parity to RCD (RCD-based systems)

IO Type	Interface	Pin	Description
O	DDR5	M0_SA_CA[13:8]	Sub-channel A command/address bits[13:8] to DRAM (non-RCD systems)
	DDR5	M0_SA_CA_CP[13:0]	Package Option: Copy of Sub-channel A command/address bits
O	DDR5	M0_SB_CA[6:0]	Sub-channel B command/address bits[6:0] to DRAM (non-RCD systems) Sub-channel B command/ Address to RCD (RCD-based systems)
O	DDR5	M0_SB_CA7/M0_SB_DPAR	Sub-channel B command/address bit[7] to DRAM (non-RCD systems) Sub-channel B command/address parity to RCD (RCD-based systems)
O	DDR5	M0_SB_CA[13:8]	Sub-channel B command/address bits[13:8] to DRAM (non-RCD systems)
O	DDR5	M0_SB_CA_CP[13:0]	Package Option: Copy of Sub-channel B command/address bits
O	DDR5		
I/O	DDR5	M0_SA_DQ[31:0]	Sub-channel A Data bits
I/O	DDR5	M0_SA_CB[7:0]	Sub-channel A ECC/Check bits
I/O	DDR5	M0_SA_DQS{9:0}_t, M0_SA_DQS{9:0}_c	Sub-channel A Differential Data Strokes
I/O	DDR5	M0_SB_DQ[31:0]	Sub-channel B Data bits
I/O	DDR5	M0_SB_CB[7:0]	Sub-channel B ECC/Check bits
I/O	DDR5	M0_SB_DQS{9:0}_t, M0_SB_DQS{9:0}_c	Sub-channel B Differential Data Strokes
I	DDR5	M0_ALERT_n	DRAM/DIMM parity error alert
O	DDR5	M0_RESET_n	DRAM/DIMM asynchronous reset
I/O	DDR5	M0_ALERT_n_B	DRAM parity error alert for DDR5 sub-channel B on EDSFF

IO Type	Interface	Pin	Description
O	DDR5	M0_RESET_n_B	DRAM asynchronous reset for DDR5 sub-channel B
A	DDR5	M0_ZQCAL	Reference pin for ZQ calibration of controller's DDR interface
I	DDR5	M0_LBDQ [1:0]	Loopback data from RCD.
I	DDR5	M0_LBDQS [1:0]	Loopback strobe from RCD.
I/O	DDR5	PGOOD_DDR / PCAMP	PGOOD_DDR is UDIMM Only. Reports PWR_GOOD for PMIC5100.
O	DDR5	TEN	
I/O	DDR5	DDR_ATO	
I/O	DDR5	DDR_DTO	
O	DDR4	M0_CKA_t, M0_CKA_c, M0_CKB_t, M0_CKB_c	Differential output clocks to DRAM/DIMM.
O	DDR4	M0_CKC_t, M0_CKC_c, M0_CKD_t, M0_CKD_c	Differential output clocks to DRAM/DIMM
O	DDR4	M0_CS0_n, M0_CS1_n, M0_CS2_n, M0_CS3_n	Chip Select for each supported rank
O	DDR4	M0_CKE0, M0_CKE1, M0_CKE2, M0_CKE3	Clock Enable for each supported rank
O	DDR4	M0_ODT0, M0_ODT1, M0_ODT2, M0_ODT3	On-die Termination enable for each supported rank
O	DDR4	M0_ACT_n	Activate command signal
O	DDR4	M0_A[17,13,11,9:0]	Address pins, not including dual-purpose address/command pins.
O	DDR4	M0_RAS_n/M0_A16	Dual purpose Row Address Strobe and A16
	DDR4	M0_CAS_n/M0_A15	Dual purpose Column Address Strobe and A15
O	DDR4	M0_WE_n/M0_A14	Dual purpose Write Enable and A14

IO Type	Interface	Pin	Description
	DDR4	M0_BC_n/M0_A12	Dual purpose Burst Chop and A12
O	DDR4	M0_AP/M0_A10	Dual purpose Auto Precharge and A10
O	DDR4	M0_PAR	Command/address parity input
O	DDR4	M0_BG[1:0]	Bank Group signals
O	DDR4	M0_BA[1:0]	Bank Address signals
O	DDR4	M0_CID[2:0]	Chip ID signals
I/O	DDR4	M0_DQ[63:0]	Data bits
I/O	DDR4	M0_CB[7:0]	ECC/Check bits
I/O	DDR4	M0_DQS{17:0}_t, M0_DQS{17:0}_c	Differential Data Strobes
I	DDR4	M0_ALERT_n	DRAM/DIMM parity error alert
O	DDR4	M0_RESET_n	DRAM/DIMM asynchronous reset
A	DDR4	M0_ZQCAL	Reference pin for ZQ calibration of controller's DDR interface
I	DDR4	M0_EVENT_n	Thermal event signal from DDR4 SPD Hub.
A	DDR4	M0_VrefCA	
I	CXL	PECLK_t, PECLK_n	Differential PCIe Reference Clock
I	CXL	PERX{7:0}_p, PERX{7:0}_n	Differential PCIe Receiver signals
O	CXL	PETX{7:0}_p, PETX{7:0}_n	Differential PCIe Transmitter signals
I	CXL	PERST_n	PCIe Reset.
I	I3C Host	HSCL	Host I2C/I3C Clock
I/O	I3C Host	HSDA	Host I2C/I3C Data
O	I3C Host	MSCL	Memory Card I2C/I3C Clock
I/O	I3C Host	MSDA	Memory Card I2C/I3C Data

IO Type	Interface	Pin	Description
I	UART	RXD	UART Receiver
O	UART	TXD	UART Transmitter
O	SPI	SCLK	SPI Clock signal
O	SPI	SCS_n	SPI Chip Select signal
I/O	SPI	SIO[3:0]	SPI Data
I	JTAG	TRST_n	TAP Controller asynchronous reset
I	JTAG	TCK	Test Clock
I	JTAG	TMS	Test Mode Select
I	JTAG	TDI	Test Scan Data In
O	JTAG	TDO	Test Scan Data Out
I	JTAG	TMUXSEL[1:0]	Select scan chain target: b00 - uController Debug b01 - PCIe Physical b1x - Reserved
I/O	GPIO	GPIO[7:0]	General Purpose IOs
O	GPIO	LED[2:0]	Status LEDs (Definition TBD)
I	Misc.	PWRDIS	Card 12V shutoff indicator in EDSFF spec
I	Misc.	PGOOD / RESET_n	Controller input power system stable / Release controller from reset
I	Misc.	REFCLK_p, REFCLK_n (Single Ended CLK Option: EXT_OSC_CLK)	Differential Controller input clock Option: Single Ended CLK Input
I	Misc.	CLKSEL [1:0]	PLL Reference Clock Source: 0 - PECLK0_p/n 1 - REFCLK_p/n

IO Type	Interface	Pin	Description
<i>I</i>	<i>Misc.</i>	<i>RSTSEL[1:0]</i>	Select primary reset source: <i>b00</i> - <i>PERST0_n</i> & <i>PERST1_n</i> <i>b01</i> - <i>PGOOD (RESET_n)</i> <i>b10</i> - <i>PGOOD (RESET_n)</i> & <i>PERST0_n</i> & <i>PERST1_n</i> <i>b11</i> - Reserved
<i>I</i>	<i>Misc.</i>	<i>BOOTSEL[1:0]</i>	Select internal CPU boot mode: <i>b00</i> - Local ROM <i>b01</i> - Local RAM <i>b10</i> - Reserved <i>b11</i> - External SPI
<i>I</i>	<i>Misc.</i>	<i>RCVRY</i>	<i>RCVRY</i> pin
<i>I</i>	<i>Misc.</i>	<i>Vendor_Specific [9:8]</i>	
<i>I/O</i>	<i>Misc.</i>	<i>DEBUG[3:0]</i>	Vendor specific debug pins

10 Appendix A

This appendix contains example ball maps for informational purposes.

10.1 Scope

The proposed x8 CMC01 package standard was specifically created for CXL (x8) memory controllers used in a form factor where embedded DRAM components serve as the memory media, and no RCDs are integrated within. The x8 CMC01 standard package is a 19x19 mm² 0.7 mm pitch 27x27 ball array package.

The DDR4 and DDR5 are the two use cases for the x8 CMC01 standard package. There's a separate ball map for each use case.

10.2 Summary of the x8 CMC01 Package Balls

This proposed ballout accommodates almost all the functional signals, with the following exceptions.

- Three extra pins, HSA[2:0], are added for default SMBus/I2C/I3C address on the host side.
- The PERES pin is added in this proposal for PCIe reference resistor.
- The SMRSTN pin is added for sideband system management reset on the EDSFF module.
- These signals, M0_ALERT_n_B, LED[2], GPIO[7], RCVRY and PWRDIS are not used in this proposed package.

10.3 Reference #1 DDR5 Use Case Ball Map

The proposed ball map is shown in **Figure 11 — Reference #1 Proposed Ball Map for DDR5 Use Cases.**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27		
A	Vss	MO_SA,C A,CP6	Vss	MO_SA,C A,CP9	Vss	MO_SA,C S1,n	MO_SA,C KC,c	Vss	MO_SA,C KA,c	Vss	MO_SA,C KD,c	Vss	MO_SA,C KB,c	Vss	MO_SB,C KB,c	Vss	MO_SB,C KD,c	Vss	MO_SB,C KA,c	Vss	MO_SB,C KC,c	MO_SB,C S1,n	Vss	MO_SB,C A,CP6	Vss	MO_SB,C A,CP7	Vss		
B	MO_SA,C A,CP2	Vss	MO_SA,C A,CP12	Vss	MO_SA,C S3,n	Vss	MO_SA,C KC,1	Vss	MO_SA,C KA,1	Vss	MO_SA,C KD,1	Vss	MO_SA,C KB,1	Vss	MO_SB,C KB,1	Vss	MO_SB,C KD,1	Vss	MO_SB,C KA,1	Vss	MO_SB,C KC,1	Vss	MO_SB,C S3,n	Vss	MO_SB,C A,CP13	Vss	MO_SB,C A,CP5		
C	Vss	MO_SA,C A,CP0	Vss	MO_SA,C A,CP7	Vss	MO_SA,C A,CP11	Vss	MO_SA,C A0	Vss	MO_SA,C A6	Vss	MO_SA,C A12	Vss	MO_SB,C A11	Vss	MO_SB,C A13	Vss	MO_SB,C A7	Vss	MO_SB,C A1	Vss	MO_SB,C A5	Vss	MO_SB,C A,CP2	Vss	MO_SB,C A,CP9	Vss		
D	MO_SA,C A,CP4	Vss	MO_SA,C A,CP8	Vss	MO_SA,C A,CP5	Vss	MO_SA,C A4	Vss	MO_SA,C A2	Vss	MO_SA,C A8	Vss	MO_SA,C A10	Vss	MO_SB,C A12	Vss	MO_SB,C A9	Vss	MO_SB,C A3	Vss	MO_SB,C A,CP10	Vss	MO_SB,C A,CP0	Vss	MO_SB,C A,CP1	Vss	MO_SB,C A,CP5		
E	Vss	MO_SA,C S0,n	Vss	MO_SA,C A,CP10	Vss	MO_SA,C A,CP13	Vss	MO_SA,C A,CP13	Vss	MO_SA,C A3	Vss	MO_SA,C A9	Vss	MO_SA,C A11	Vss	MO_SB,C A8	Vss	MO_SB,C A2	Vss	MO_SB,C A,CP12	Vss	MO_SB,C A,CP12	Vss	MO_SB,C A,CP11	Vss	MO_SB,C S0,n	Vss		
F	Vss	Vss	MO_SA,C B4	Vss	MO_SA,C B5	Vss	MO_SA,C A,CP5	Vss	MO_SA,C A5	Vss	MO_SA,C A7	Vss	MO_SA,C A13	Vss	MO_SB,C A10	Vss	MO_SB,C A9	Vss	MO_SB,C A4	Vss	MO_SB,C A,CP4	Vss	MO_SB,C B5	Vss	MO_SB,C B4	Vss	Vss		
G	MO_SA,D Q59,c	MO_SA,D Q59,1	Vss	MO_SA,C B6	Vss	MO_SA,C B7	Vss	MO_SA,C S2,n	Vss	MO_SA,C A1	Vss	MO_RESE T,n	Vss	MO_ALER T,n	Vss	MO_RESE T,n,B	Vss	MO_SB,C A0	Vss	MO_SB,C S2,n	Vss	MO_SB,C B7	Vss	MO_SB,C B6	Vss	MO_SB,D Q59,1	MO_SB,D Q59,c		
H	Vss	Vss	MO_SA,C B3	Vss	MO_SA,C B1	Vss	MO_LBDO S0	Vss	MO_LBDO S0	Vss	DDR_ATO	Vss	Vss	MO_ZOCLA L	Vss	DDR_DTO	TEN	Vss	MO_LBDO S1	Vss	MO_LBDO S1	Vss	MO_SB,C B1	Vss	MO_SB,C B3	Vss	Vss		
J	MO_SA,D Q54,c	MO_SA,D Q54,1	Vss	MO_SA,C B2	Vss	MO_SA,C B0	Vss	Vddq	Vddq	Vss	Vddq	Vss	Vss	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	MO_SB,C B0	Vss	MO_SB,C B2	Vss	MO_SB,D Q54,1	MO_SB,D Q54,c	
K	Vss	Vss	MO_SA,D Q28	Vss	MO_SA,D Q29	Vss	SIO1	Vss		Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq		Vss	BOOTSEL 0	Vss	MO_SB,D Q5	Vss	MO_SB,D Q4,B	Vss	Vss		
L	MO_SA,D Q58,c	MO_SA,D Q58,1	Vss	MO_SA,D Q30	Vss	MO_SA,D Q31	Vss	Vddq	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	MO_SB,D Q7,B	Vss	MO_SB,D Q6,B	Vss	MO_SB,D Q55,1	MO_SB,D Q55,c	
M	Vss	Vss	MO_SA,D Q27	Vss	MO_SA,D Q25	Vss	SIO3	Vddq				Vddq	Vss	Vddq	Vss	Vddq,qpl				Vddq	DEBU02	Vss	MO_SB,D Q1,B	Vss	MO_SB,D Q3,B	Vss	Vss		
N	MO_SA,D Q53,c	MO_SA,D Q53,1	Vss	MO_SA,D Q26	Vss	MO_SA,D Q24	Vss	SIO2	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	DEBU03	Vss	MO_SB,D Q0,B	Vss	MO_SB,D Q2,B	Vss	MO_SB,D Q50,1	MO_SB,D Q50,c
P	Vss	Vss	MO_SA,D Q20	Vss	MO_SA,D Q21	Vss	SIO0	SCS,n	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	MSDA	LED0	Vss	MO_SB,D Q13,B	Vss	MO_SB,D Q12,B	Vss	Vss		
R	MO_SA,D Q57,c	MO_SA,D Q57,1	Vss	MO_SA,D Q22	Vss	MO_SA,D Q23	Vss	TXD	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	RSTSEL0	Vss	MO_SB,D Q15,B	Vss	MO_SB,D Q14,B	Vss	MO_SB,D Q56,1	MO_SB,D Q56,c
T	Vss	Vss	MO_SA,D Q19	Vss	MO_SA,D Q17	Vss	SCLK	RXD	Vendor_Sp ecifc0	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	HSDA	HSCL	BOOTSEL 1	Vss	MO_SB,D Q9,B	Vss	MO_SB,D Q11,B	Vss	Vss	
U	MO_SA,D Q52,c	MO_SA,D Q52,1	Vss	MO_SA,D Q18	Vss	MO_SA,D Q16	Vss	GPIO2	TCK	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	MSCL	PERST,n	Vss	MO_SB,D Q8,B	Vss	MO_SB,D Q10,B	Vss	MO_SB,D Q51,1	MO_SB,D Q51,c		
V	Vss	Vss	MO_SA,D Q12	Vss	MO_SA,D Q13	Vss	Vendor_Sp ecifc1	GPIO0	PGOOD/R ESET,n	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	CLKSEL0	RSTSEL1	LED1	Vss	MO_SB,D Q21,B	Vss	MO_SB,D Q20,B	Vss	Vss	
W	MO_SA,D Q56,c	MO_SA,D Q56,1	Vss	MO_SA,D Q14	Vss	MO_SA,D Q15	Vss	GPIO6	Vdd18	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vdd18	DEBU01	Vss	MO_SB,D Q23,B	Vss	MO_SB,D Q22,B	Vss	MO_SB,D Q57,1	MO_SB,D Q57,c		
Y	Vss	Vss	MO_SA,D Q11	Vss	MO_SA,D Q9	Vss	GPIO3	TDI	TRST,n	Vddq	Vss	Vddq				Vddq	Vss	Vddq	EXT_OSC CLK	Vss	CLKSEL1	Vss	MO_SB,D Q17,B	Vss	MO_SB,D Q19,B	Vss	Vss		
AA	MO_SA,D Q51,c	MO_SA,D Q51,1	Vss	MO_SA,D Q10	Vss	MO_SA,D Q8	Vss	TMS	TDO	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss			Vddq	Vendor_Sp ecifc10	Vss	MO_SB,D Q16,B	Vss	MO_SB,D Q18,B	Vss	MO_SB,D Q52,1	MO_SB,D Q52,c		
AB	Vss	Vss	MO_SA,D Q4	Vss	MO_SA,D Q5	Vss	Vss	GPIO4	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	SMRST,n	Vss	Vss	MO_SB,D Q29,B	Vss	MO_SB,D Q28,B	Vss	Vss		
AC	MO_SA,D Q55,c	MO_SA,D Q55,1	Vss	MO_SA,D Q6	Vss	Vss	PETX0_P	Vss	PETX1_P	Vss	PETX2_P	Vss	PETX3_P	Vss	PETX4_P	Vss	PETX5_P	Vss	PETX6_P	Vss	PETX7_P	Vss	Vss	MO_SB,D Q30,B	Vss	MO_SB,D Q58,1	MO_SB,D Q58,c		
AD	Vss	Vss	MO_SA,D Q3	Vss	MO_SA,D Q7	Vss	PETX0_N	Vss	PETX1_N	Vss	PETX2_N	Vss	PETX3_N	Vss	PETX4_N	Vss	PETX5_N	Vss	PETX6_N	Vss	PETX7_N	Vss	Vss	MO_SB,D Q31,B	Vss	MO_SB,D Q27,B	Vss	Vss	
AE	MO_SA,D Q50,c	MO_SA,D Q50,1	Vss	MO_SA,D Q1	Vss	MO_SA,D Q2	Vss	Vss	Vss	Vss	Vss	Vss	Vss	PERES	Vss	Vss	Vss	Vss	Vss	Vss	Vss	MO_SB,D Q29,B	Vss	MO_SB,D Q28,B	Vss	MO_SB,D Q53,1	MO_SB,D Q53,c		
AF	DEBU00	Vss	Vendor_Sp ecifc9	Vss	MO_SA,D Q0	Vss	PERX0_P	Vss	PERX1_P	Vss	PERX2_P	Vss	PERX3_P	Vss	PERX4_P	Vss	PERX5_P	Vss	PERX6_P	Vss	PERX7_P	Vss	MO_SB,D Q24,B	Vss	Vendor_Sp ecifc12	Vendor_Sp ecifc11	Vendor_Sp ecifc11		
AG	Vss	GPIO5	PECLK,1	PECLK,n	Vss	Vss	PERX0_N	Vss	PERX1_N	Vss	PERX2_N	Vss	PERX3_N	Vss	PERX4_N	Vss	PERX5_N	Vss	PERX6_N	Vss	PERX7_N	Vss	Vss	GPIO1	PGOOD_DD RPCAMP	Vendor_Sp ecifc8	Vss		

Figure 11 — Reference #1 Proposed Ball Map for DDR5 Use Cases

10.4 Reference #2 DDR4 Use Case Ball Map

The proposed ball map is shown in **Figure 12 — Reference #2 Proposed Ball Map for DDR4 Use Cases.**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27			
A	Vss	MD_A3	Vss		Vss	MD_OKE1		Vss		Vss	MD_OKE2	Vss	MD_OKA_2	Vss	MD_OKE2	Vss	MD_OKE2	Vss		Vss		MD_CS1_n	Vss	MD_OAS_n MD_A19	Vss		Vss			
B	MD_A1	Vss	MD_A6	Vss	MD_OKE3	Vss		Vss		Vss	MD_OKE3	Vss	MD_OKA_1	Vss	MD_OKE3	Vss	MD_OKE3	Vss		Vss		Vss	MD_CS3_n	Vss		Vss				
C	Vss	MD_ACT_n	Vss		Vss		Vss	MD_A7	Vss	MD_BC_n MD_A12	Vss	MD_B01	Vss		Vss	MD_ODT3	Vss	MD_CD2	Vss		Vss		Vss	MD_A10	Vss		Vss			
D	MD_A2	Vss	MD_A4	Vss		Vss	MD_A9	Vss	MD_A8	Vss	MD_A11	Vss	MD_B00	Vss	MD_ODT2	Vss	MD_ODT0	Vss	MD_APMD _A10	Vss	MD_RAS_n MD_A18	Vss	MD_A0	Vss		Vss				
E	Vss	MD_OKE2	Vss	MD_A5	Vss		Vss		Vss		Vss		Vss		Vss		Vss	MD_BA1	Vss	MD_A17	Vss	MD_WE_n MD_A14	Vss	MD_PAS	Vss	MD_CS2_n	Vss			
F	Vss	Vss	MD_CB4	Vss	MD_CB5	Vss		Vss		Vss		Vss		Vss	MD_ODT1	Vss	MD_CD1	Vss	MD_CD0	Vss		MD_A13	Vss		Vss		Vss			
G	MD_DQS17_c	MD_DQS17_j	Vss	MD_CB6	Vss	MD_CB7	Vss	MD_OKE2	Vss		Vss	MD_RESET_n	Vss	MD_ALERT_n	Vss		Vss	MD_BA0	Vss	MD_CS2_n	Vss		Vss		Vss					
H	Vss	Vss	MD_CB3	Vss	MD_CB1	Vss		Vss		Vss		Vss	Vss	MD_ZQCAL	Vss		TEN	Vss		Vss		Vss		Vss		Vss	Vss			
J	MD_DQS8_c	MD_DQS8_j	Vss	MD_CB2	Vss	MD_CB0	Vss	Vddq	Vddq	Vss	Vddq	Vss	Vss	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss		Vss		Vss				
K	Vss	Vss	MD_DQ28	Vss	MD_DQ29	Vss	SIO1	Vss		Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq		Vss	BOOTSEL0	Vss	MD_DQ37_B	Vss	MD_DQ36_c	Vss	Vss			
L	MD_DQS12_c	MD_DQS12_j	Vss	MD_DQ30	Vss	MD_DQ31	Vss	Vddq	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	MD_DQ39_B	Vss	MD_DQ38_B	Vss	MD_DQS13_j	MD_DQS13_c		
M	Vss	Vss	MD_DQ27	Vss	MD_DQ25	Vss	SIO3	Vddq				Vddq	Vss	Vddq	Vss	Vddq	pll			Vddq	DEBU02	Vss	MD_DQ33_B	Vss	MD_DQ35_c	Vss	Vss			
N	MD_DQS3_c	MD_DQS3_j	Vss	MD_DQ28	Vss	MD_DQ24	Vss	SIO2	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	DEBU03	Vss	MD_DQ32_B	Vss	MD_DQ34_B	Vss	MD_DQ34_c	MD_DQ34_c			
P	Vss	Vss	MD_DQ20	Vss	MD_DQ21	Vss	SIO0	SCS_n	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	MSDA	LED0	Vss	MD_DQ45_B	Vss	MD_DQ44_B	Vss	Vss			
R	MD_DQS11_c	MD_DQS11_j	Vss	MD_DQ22	Vss	MD_DQ23	Vss	TXD	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	RSTSEL0	Vss	MD_DQ47_B	Vss	MD_DQ46_B	Vss	MD_DQS14_j	MD_DQS14_c			
T	Vss	Vss	MD_DQ16	Vss	MD_DQ17	Vss	SCLK	RXD	Vendor_Specific0	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	HSDA	HSCL	BOOTSEL1	Vss	MD_DQ41_B	Vss	MD_DQ43_B	Vss	Vss			
U	MD_DQS2_c	MD_DQS2_j	Vss	MD_DQ18	Vss	MD_DQ19	Vss	GPIO2	TCK	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	MSCL	PERST_n	Vss	MD_DQ40_B	Vss	MD_DQ42_B	Vss	MD_DQ55_c	MD_DQ55_c			
V	Vss	Vss	MD_DQ12	Vss	MD_DQ13	Vss	Vendor_Specific1	GPIO0	PGOOD/RESET_n	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	CLKSEL0	RSTSEL1	LED1	Vss	MD_DQ53_B	Vss	MD_DQ52_B	Vss	Vss			
W	MD_DQS10_c	MD_DQS10_j	Vss	MD_DQ14	Vss	MD_DQ15	Vss	GPIO6	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	DEBU01	Vss	MD_DQ55_B	Vss	MD_DQ54_B	Vss	MD_DQS15_j	MD_DQS15_c
Y	Vss	Vss	MD_DQ11	Vss	MD_DQ9	Vss	GPIO3	TDI	TRST_n	Vddq	Vss	Vddq			Vddq	Vss	Vddq	EXT_OSC_CLK	Vss	CLKSEL1	Vss	MD_DQ49_B	Vss	MD_DQ51_B	Vss	Vss				
AA	MD_DQS1_c	MD_DQS1_j	Vss	MD_DQ10	Vss	MD_DQ8	Vss	TMS	TDO	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss		Vddq	Vendor_Specific10	Vss	MD_DQ48_B	Vss	MD_DQ50_B	Vss	MD_DQ58_c	MD_DQ58_c				
AB	Vss	Vss	MD_DQ4	Vss	MD_DQ5	Vss	Vss	GPIO4	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	Vddq	Vss	SMRST_n	Vss	Vss	MD_DQ51_B	Vss	MD_DQ50_B	Vss	Vss			
AC	MD_DQS9_c	MD_DQS9_j	Vss	MD_DQ6	Vss	Vss	PETX0_P	Vss	PETX1_P	Vss	PETX2_P	Vss	PETX3_P	Vss	PETX4_P	Vss	PETX5_P	Vss	PETX6_P	Vss	PETX7_P	Vss	Vss	MD_DQ30_B	Vss	MD_DQS16_j	MD_DQS16_c			
AD	Vss	Vss	MD_DQ3	Vss	MD_DQ7	Vss	PETX0_N	Vss	PETX1_N	Vss	PETX2_N	Vss	PETX3_N	Vss	PETX4_N	Vss	PETX5_N	Vss	PETX6_N	Vss	PETX7_N	Vss	MD_DQ53_B	Vss	MD_DQ55_c	Vss	Vss			
AE	MD_DQS0_c	MD_DQS0_j	Vss	MD_DQ1	Vss	MD_DQ2	Vss	Vss	Vss	Vss	Vss	Vss	Vss	PERES	Vss	Vss	Vss	Vss	Vss	Vss	Vss	MD_DQ56_B	Vss	MD_DQ57_B	Vss	MD_DQ57_c	MD_DQ57_c			
AF	DEBU00	Vss	Vendor_Specific9	Vss	MD_DQ0	Vss	PERX0_P	Vss	PERX1_P	Vss	PERX2_P	Vss	PERX3_P	Vss	PERX4_P	Vss	PERX5_P	Vss	PERX6_P	Vss	PERX7_P	Vss	MD_DQ58_B	Vss	Vendor_Specific12	Vss	Vendor_Specific11			
AG	Vss	GPIO5	PECLK_1	PECLK_n	Vss	Vss	PERX0_N	Vss	PERX1_N	Vss	PERX2_N	Vss	PERX3_N	Vss	PERX4_N	Vss	PERX5_N	Vss	PERX6_N	Vss	PERX7_N	Vss	Vss	GPIO1	PS000_D0 N/C/06P	Vendor_Specific8	Vss			

Figure 12 — Reference #2 Proposed Ball Map for DDR4 Use Cases

11 Appendix B

This appendix contains example ball maps for informational purposes.

11.1 Ball Map Use Cases

The x8 CMC01 Large Pitch Package is a 19x19 mm² 0.8 mm pitch 23x23 ball array.

The DDR4 and DDR5 are the two use cases for the x8 CMC01 Large Pitch Package; there is a separate ball map for each use case.

11.2 Reference #3 DDR5 Use Case Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
A	VSS	M0_SA_DQ55_f	VSS	VSS	M0_SB_DQ55_f	M0_SB_DQ24	VSS	M0_SB_DQ18	M0_SA_DQ56_f	M0_SB_DQ22	M0_SB_DQ26	M0_SA_DQ57_f	M0_SB_DQ30	VSS	M0_SB_DQ30	M0_SB_DQ27_f	M0_SA_DQ57_f	M0_SB_DQ26	M0_SB_DQ22	M0_SB_DQ56_f	M0_SB_DQ18	VSS	M0_SB_DQ24	M0_SB_DQ55_f	VSS	VSS	M0_SB_DQ55_f	VSS	VSS	M0_SA_DQ54_f	VSS		
B	M0_SB_DQ30	M0_SA_DQ55_f	M0_SB_DQ9	VDDQ	M0_SB_DQ55_f	M0_SB_DQ13	VSS	M0_SB_DQ19	M0_SA_DQ56_f	M0_SB_DQ21	M0_SB_DQ27	M0_SA_DQ57_f	M0_SB_DQ29	VSS	M0_SB_DQ29	M0_SB_DQ57_f	M0_SA_DQ57_f	M0_SB_DQ21	M0_SB_DQ56_f	M0_SB_DQ19	VSS	M0_SB_DQ13	M0_SB_DQ55_f	VDDQ	M0_SB_DQ9	M0_SB_DQ55_f	M0_SB_DQ9	M0_SA_DQ54_f	M0_SB_DQ30				
C	M0_SB_DQ11	VSS	M0_SB_DQ8	VSS	VDDQ	M0_SB_DQ12	VSS	VSS	M0_SB_DQ17	VSS	M0_SB_DQ20	VSS	M0_SB_DQ25	VSS	M0_SB_DQ28	VSS	M0_SB_DQ28	VSS	M0_SB_DQ25	VSS	M0_SB_DQ20	VSS	M0_SB_DQ12	VDDQ	VSS	VSS	M0_SB_DQ8	VSS	M0_SB_DQ11				
D	M0_SB_DQ5	M0_SB_DQ5	M0_SB_DQ4	VDDQ	M0_SB_DQ15	VDDQ	VSS	M0_SB_DQ16	VDDQ	M0_SB_DQ23	VDDQ	M0_SB_DQ24	VDDQ	M0_SB_DQ31	VDDQ	VSS	VDDQ	M0_SB_DQ31	VDDQ	M0_SB_DQ23	VDDQ	M0_SB_DQ16	VSS	VDDQ	M0_SB_DQ15	VDDQ	M0_SB_DQ4	M0_SB_DQ5	M0_SB_DQ5	M0_SB_DQ6			
E	M0_SB_DQ54_f	M0_SB_DQ54_f	VSS	M0_SB_DQ7	M0_SB_C_S2_n	VSS	M0_SB_C_S1_n	M0_SB_C_S0_n	M0_RESE_T_n	M0_ZQCAL	RSVD_U_O_NOT_CONNECTED	RSVD_U_O_NOT_CONNECTED	TEN	BOOTSEL_0	BOOTSEL_1	BTSEL0	BTSEL1	THERM_PAD0	PWR_EN	RSVD_U_O_NOT_CONNECTED	RSVD_U_O_NOT_CONNECTED	M0_ZQCAL	M0_RESE_T_n	M0_SB_C_S0_n	M0_SB_C_S1_n	VSS	M0_SB_C_S2_n	M0_SB_DQ7	VSS	M0_SB_DQ54_f			
F	M0_SB_DQ54_f	M0_SA_DQ54_f	M0_SB_DQ1	VDDQ	M0_SB_C_A3	M0_SB_C_A1	VSS	M0_SB_C_S3_n	M0_EVE_NT_n	VSS	M0_DLB_DQ	RCVRY	SAVE_N	CLKSEL	VSS	PWRDQ0	THERM_PAD0	VSS	M0_DLB_DQ5	M0_DLB_DQ	VSS	M0_SB_C_S3_n	M0_SB_C_A1	M0_SB_C_A3	VDDQ	M0_SB_DQ1	M0_SA_DQ54_f	M0_SB_DQ5	M0_SA_DQ54_f				
G	M0_SB_DQ2	M0_SB_DQ3	VSS	M0_SB_DQ0	M0_SB_C_A9	VSS	M0_SB_C_A7/M0_S_B_DPAR	M0_SB_C_A5	M0_Vref_A	LED1	LED2	RCVRY	PCAMP	FAIL_N	VD018	GPIO7	VD018	GPIO6	PGOOD_DDR/PCAMP	GPIO5	GPIO4	GPIO3	M0_Vref_A	M0_SB_C_A5	M0_SB_C_A7/M0_S_B_DPAR	VSS	M0_SB_C_A9	M0_SB_DQ0	VSS	M0_SB_DQ2			
H	M0_SB_C_B6	M0_SB_C_B5	M0_SB_C_B4	VDDQ	M0_SB_C_A13	M0_SB_C_A11	VSS	M0_SB_C_A0	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VD018	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	M0_SB_C_A0	VSS	M0_SB_C_A11	M0_SB_C_A13	VDDQ	M0_SB_C_B4	M0_SB_C_B5	M0_SB_C_B6
J	M0_SB_DQ59_f	M0_SB_DQ59_f	VSS	M0_SB_C_B7	VSS	VSS	M0_SB_C_A4	M0_SB_C_A2	LED0	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	GPIO2	M0_SB_C_A2	M0_SB_C_A4	VSS	VSS	M0_SB_C_B7	VSS	M0_SB_DQ59_f	M0_SB_DQ59_f		
K	M0_SA_DQ59_f	M0_SB_C_B1	VDDQ	M0_SA_C_KB_f	M0_SA_C_KB_f	VSS	M0_SB_C_A6	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VD018	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	M0_SA_C_KB_f	M0_SA_C_KB_f	VDDQ	M0_SB_C_B1	M0_SA_DQ59_f		
L	M0_SB_C_B2	M0_SB_C_B3	VSS	M0_SB_C_B0	VSS	VSS	M0_SB_C_A8	M0_SB_C_A10	DEBUG3	VSS	VDDQ	VSS	VDDQ	VSS	VSS	VSS	VDDC	VSS	VDDQ	VSS	VDDQ	VSS	GPIO1	M0_SB_C_A10	M0_SB_C_A8	VSS	VSS	M0_SB_C_B0	VSS	M0_SB_C_B2			
M	M0_SA_C_B6	M0_SA_C_B5	M0_SA_C_B4	VDDQ	M0_SB_C_KB_f	M0_SB_C_KB_f	VSS	M0_SB_C_A12	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VD018	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	M0_SB_C_A12	M0_SB_C_KB_f	M0_SB_C_KB_f	VDDQ	M0_SA_C_B4	M0_SA_C_B5	M0_SA_C_B6			
N	M0_SB_DQ58_f	M0_SB_DQ58_f	VSS	M0_SA_C_B7	VSS	VSS	DDRR0_A0_DIN_NC_P_A7/M0_S_B_DPAR	DDRR0_CS_DIN_NC_P_A7/M0_S_B_DPAR	DEBUG2	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	GPIO0	DDRR1_C5_DIN_NC_P_A7/M0_S_B_DPAR	DDRR1_A0_DIN_NC_P_A7/M0_S_B_DPAR	VSS	VSS	M0_SA_C_B7	VSS	M0_SB_DQ58_f	M0_SB_DQ58_f		
P	M0_SA_DQ58_f	M0_SA_DQ58_f	VSS	VSS	DDRR0_A0_DIN_NC_P_A7/M0_S_B_DPAR	DDRR0_CS_DIN_NC_P_A7/M0_S_B_DPAR	VSS	M0_ALER_T_n	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	M0_ALER_T_n	DDRR1_A0_DIN_NC_P_A7/M0_S_B_DPAR	VSS	VSS	VSS	VSS	M0_SA_C_B1	M0_SA_DQ58_f		
R	M0_SA_C_B2	M0_SA_C_B3	VSS	M0_SA_C_B0	M0_SA_C_KA_f	M0_SA_C_KA_f	VSS	M0_SA_C_A12	DEBUG1	VSS	VDDQ	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDA	VSS	VDDQ	VSS	EVENT_N	M0_SA_C_A12	VSS	M0_SA_C_KA_f	M0_SA_C_KA_f	M0_SA_C_B0	VSS	M0_SA_C_B3	M0_SA_C_B2		
T	M0_SA_DQ30	M0_SA_DQ29	M0_SA_DQ28	VDDQ	VSS	VSS	M0_SA_C_A10	M0_SA_C_A8	VSS	VDDQ	VSS	VDDC	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	M0_SA_C_A8	M0_SA_C_A10	VSS	VSS	VDDQ	M0_SA_DQ28	M0_SA_DQ29	M0_SA_DQ30		
U	M0_SB_DQ53_f	M0_SB_DQ53_f	VSS	M0_SB_C_KA_f	M0_SB_C_KA_f	VSS	M0_SA_C_A6	DEBUG0	VSS	VDDQ	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	M0_SA_C_A6	VSS	M0_SB_C_KA_f	M0_SB_C_KA_f	VSS	M0_SB_DQ53_f	M0_SB_DQ53_f			
V	M0_SA_DQ53_f	M0_SA_DQ53_f	M0_SA_DQ25	VDDQ	VSS	VSS	M0_SA_C_A4	M0_SA_C_A2	VSS	RSVD_U_O_NOT_CONNECTED	RSVD_U_O_NOT_CONNECTED	VDDC	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VD010	VSS	MSDA	HSLC	M0_SA_C_A2	M0_SA_C_A4	VSS	VSS	VDDQ	M0_SA_DQ25	M0_SA_DQ53_f	
W	M0_SA_DQ26	M0_SA_DQ27	VSS	M0_SA_DQ24	M0_SA_C_A13	M0_SA_C_A11	VSS	M0_SA_C_A0	VDD18	VSS	VDDA	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VD018	MSCL	HSDA	M0_SA_C_A0	VSS	M0_SA_C_A11	M0_SA_C_A13	M0_SA_DQ24	M0_SA_DQ26		
Y	M0_SA_DQ22	M0_SA_DQ21	M0_SA_DQ20	VDDQ	M0_SA_C_A9	VSS	M0_SA_C_A5	VSS	VD018	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VD018	VSS	M0_SA_C_A5	M0_SA_C_A7/M0_S_B_DPAR	VSS	M0_SA_C_A9	VDDQ	M0_SA_DQ20	M0_SA_DQ21	M0_SA_DQ22	
AA	M0_SB_DQ52_f	M0_SB_DQ52_f	VSS	M0_SA_DQ23	M0_SA_C_A3	M0_SA_C_A1	VSS	M0_SA_C_S3_n	VDD18	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VD018	M0_SA_C_S3_n	VSS	M0_SA_C_A1	M0_SA_C_A3	M0_SA_DQ23	VSS	M0_SB_DQ52_f	M0_SB_DQ52_f		
AB	M0_SA_DQ52_f	M0_SA_DQ52_f	M0_SA_DQ17	VDDQ	M0_SA_C_S2_n	VSS	M0_SA_C_S1_n	M0_SA_C_S0_n	PGOOD/RESET_n	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	HSAD	M0_SA_C_S0_n	M0_SA_C_S1_n	VSS	M0_SA_C_S2_n	VDDQ	M0_SA_DQ17	M0_SA_DQ52_f	M0_SA_DQ52_f	
AC	M0_SA_DQ18	M0_SA_DQ19	VSS	M0_SA_DQ16	TRST_n	TAP_SEL	TDI	TMUSEL_0	TMUSEL_1	VSS	VSS	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	HSAD	HSAD	I2C_SCL	I2C_SDA	I2C_SRT_B	M0_SA_DQ16	VSS	M0_SA_DQ18	M0_SA_DQ18		
AD	M0_SA_DQ14	M0_SA_DQ13	M0_SA_DQ12	VDDQ	TDO	TCK	TMS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CLKREQ_n	RWD	VDDQ	M0_SA_DQ12	M0_SA_DQ13	M0_SA_DQ14	
AE	M0_SB_DQ51_f	M0_SB_DQ51_f	VSS	M0_SA_DQ15	VSS	VSS	VSS	PETX1_n	VSS	PETX0_n	VSS	PETX5_n	VSS	PETX7_n	VSS	VSS	PETX9_n	VSS	PETX11_n	VSS	PETX13_n	VSS	PETX15_n	VSS	PETX17_n	VSS	DUALPO_RTEN_n	TXD	M0_SA_DQ15	VSS	M0_SB_DQ51_f	M0_SB_DQ51_f	
AF	M0_SA_DQ51_f	M0_SA_DQ51_f	M0_SA_DQ9	VDDQ	REFCLK_n	VSS	PETX0_n	PETX1_p	PETX2_n	PETX3_p	PETX4_n	PETX5_p	PETX6_n	PETX7_p	VSS	PETX8_n	PETX9_p	PETX10_n	PETX11_p	PETX12_n	PETX13_p	PETX14_n	PETX15_p	VSS	PERES0	PERES1	VDDQ	M0_SA_DQ9	M0_SA_DQ51_f	M0_SA_DQ51_f			
AG	M0_SA_DQ10	M0_SA_DQ11	VSS	M0_SA_DQ8	REFCLK_p	VSS	PETX0_p	VSS	PETX2_p	VSS	PETX4_p	VSS	PETX6_p	VSS	VSS	PETX8_p	VSS	PETX10_p	VSS	PETX12_p	VSS	PETX14_p	VSS	VSS	PERST0_n	PERST1_n	M0_SA_DQ8	VSS	M0_SA_DQ10	M0_SA_DQ10			
AH	M0_SA_DQ6	M0_SA_DQ5	M0_SA_DQ4	VDDQ	PECLAD_n	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD_U_O_NOT_CONNECTED	RSVD_U_O_NOT_CONNECTED	VDDQ	M0_SA_DQ4	M0_SA_DQ6		
AJ	M0_SB_DQ50_f	M0_SB_DQ50_f	VSS	M0_SA_DQ7	VSS	VSS	PERX1_p	VSS	PERX2_p	VSS	PERX3_p	VSS	PERX5_n	VSS	PERX7_n	VSS	VSS	PERX9_p	VSS	PERX11_p	VSS	PERX13_n	VSS	PERX15_n	VSS	SIO2	SIO3	VSS	M0_SB_DQ50_f	M0_SB_DQ50_f			
AK	M0_SA_DQ50_f	M0_SA_DQ50_f	M0_SA_DQ3	VDDQ	PECLAD_n	VSS	PERX0_p	PERX1_n	PERX2_p	PERX3_p	PERX4_n	PERX5_p	PERX6_n	PERX7_p	VSS	PERX8_p	PERX9_n	PERX10_n	PERX11_p	PERX12_n	PERX13_p	PERX14_n	PERX15_p	VSS	SCS_n	SIO1	VDDQ	M0_SA_DQ3	M0_SA_DQ50_f	M0_SA_DQ50_f			
AL	VSS	M0_SA_DQ2	M0_SA_DQ0	VSS	PECLAD_f	VSS	PERX0_n	VSS	PERX2_n	VSS	PERX4_n	VSS	PERX6_n	VSS	VSS	PERX8_n	VSS	PERX10_n	VSS	PERX12_p	VSS	PERX14_p	VSS	VSS	SCLK	SIO0	M0_SA_DQ0	M0_SA_DQ2	M0_SA_DQ2	VSS			

Figure 13 — Reference #3 DDR5 Use Case Ball Map

11.2 Reference #3 DDR5 Use Case Ball Map (cont'd)**Table 47 — Reference #3 DDR5 Use Cases Pin List**

No.	Name	No.	Name	No.	Name	No.	Name
A1	VSS	B14	M0_SB_CB2	D4	VSS	E17	" M0_SA_CKB_t"
A2	M0_SA_DQS3_t	B15	VDDQ	D5	NC	E18	VSS
A3	M0_SA_DQS3_c	B16	M0_SB_CB4	D6	VSS	E19	NC
A4	VSS	B17	M0_SB_CB5	D7	M0_SA_CKA_c	E20	VSS
A5	M0_SB_DQS3_t	B18	M0_SB_DQ3	D8	VSS	E21	M0_SB_DQ9
A6	M0_SB_DQS3_c	B19	M0_SB_DQ2	D9	NC	E22	M0_SB_DQ10
A7	M0_SA_DQS8_t	B20	VDDQ	D10	VSS	E23	M0_SA_DQS5_c
A8	M0_SA_DQS8_c	B21	M0_SB_DQ4	D11	NC	F1	VSS
A9	VSS	B22	M0_SB_DQ5	D12	VSS	F2	VDDQ
A10	M0_SB_DQS8_t	B23	VDDQ	D13	BOOTSEL1	F3	VSS
A11	M0_SB_DQS8_c	C1	VSS	D14	VSS	F4	NC
A12	VSS	C2	M0_SA_DQ24	D15	BOOTSEL0	F5	VSS
A13	M0_SA_DQS9_t	C3	M0_SA_DQ25	D16	VSS	F6	NC
A14	M0_SA_DQS9_c	C4	VSS	D17	M0_SA_CKB_c	F7	VSS
A15	VSS	C5	M0_SA_DQ31	D18	VSS	F8	VDDQ
A16	M0_SB_DQS9_t	C6	M0_SA_DQ30	D19	NC	F9	VSS
A17	M0_SB_DQS9_c	C7	M0_SA_CB0	D20	VSS	F10	VDDQ
A18	M0_SA_DQS4_t	C8	M0_SA_CB1	D21	M0_SB_DQ8	F11	VSS
A19	M0_SA_DQS4_c	C9	VSS	D22	M0_SB_DQ11	F12	VSS
A20	VSS	C10	M0_SA_CB7	D23	M0_SA_DQS5_t	F13	VSS
A21	M0_SB_DQS4_t	C11	M0_SA_CB6	E1	M0_SB_DQS2_t	F14	VDDQ
A22	M0_SB_DQS4_c	C12	VSS	E2	M0_SA_DQ20	F15	VSS
A23	VSS	C13	M0_SB_CB0	E3	M0_SA_DQ23	F16	VDDQ
B1	VDDQ	C14	M0_SB_CB1	E4	VSS	F17	VSS
B2	M0_SA_DQ27	C15	VSS	E5	NC	F18	M0_SB_CA7/M0_SB_DPAR
B3	M0_SA_DQ26	C16	M0_SB_CB7	E6	VSS	F19	VSS
B4	VDDQ	C17	M0_SB_CB6	E7	M0_SA_CKA_t	F20	M0_SB_CA1
B5	M0_SA_DQ28	C18	M0_SB_DQ0	E8	VSS	F21	VSS
B6	M0_SA_DQ29	C19	M0_SB_DQ1	E9	NC	F22	VDDQ
B7	M0_SA_CB3	C20	VSS	E10	VSS	F23	VSS
B8	M0_SA_CB2	C21	M0_SB_DQ7	E11	NC	G1	M0_SA_DQS2_c
B9	VDDQ	C22	M0_SB_DQ6	E12	VSS	G2	M0_SA_DQ18
B10	M0_SA_CB4	C23	VSS	E13	NC	G3	M0_SA_DQ17
B11	M0_SA_CB5	D1	M0_SB_DQS2_c	E14	VDD18	G4	M0_SA_CA7/M0_SA_DPAR
B12	VDDQ	D2	M0_SA_DQ21	E15	NC	G5	M0_SA_CA5
B13	M0_SB_CB3	D3	M0_SA_DQ22	E16	VSS	G6	NC

Table 47 — Reference #3 DDR5 Use Cases Pin List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
G7	VDDQ	H20	M0_SB_CA4	K10	VDDC	L23	VSS
G8	VSS	H21	M0_SB_DQ14	K11	VSS	M1	M0_SA_DQS1_c
G9	VDDQ	H22	M0_SB_DQ13	K12	VDDC	M2	M0_SA_DQ10
G10	VSS	H23	M0_SB_DQS5_c	K13	VSS	M3	M0_SA_DQ9
G11	VDDQ	J1	M0_SB_DQS1_c	K14	VDDC	M4	M0_SA_CA3
G12	VSS	J2	M0_SA_DQ13	K15	VSS	M5	VSS
G13	NC	J3	M0_SA_DQ14	K16	VDDC	M6	M0_SA_CS0_n
G14	VSS	J4	NC	K17	VSS	M7	VSS
G15	VDDQ	J5	NC	K18	NC	M8	VDDQ
G16	VSS	J6	M0_SA_CA0	K19	VSS	M9	VSS
G17	VDDQ	J7	VDDQ	K20	M0_SB_CA2	M10	VDDA
G18	M0_SB_CA3	J8	VSS	K21	M0_SB_DQ17	M11	VSS
G19	NC	J9	VDDC	K22	M0_SB_DQ18	M12	VDDC
G20	NC	J10	VSS	K23	M0_SA_DQS6_c	M13	VSS
G21	M0_SB_DQ15	J11	VDD18	L1	VSS	M14	VDDC
G22	M0_SB_DQ12	J12	VSS	L2	VDDQ	M15	VSS
G23	M0_SB_DQS5_t	J13	VDDC	L3	VSS	M16	VDDA
H1	M0_SA_DQS2_t	J14	VSS	L4	M0_SA_CA4	M17	VSS
H2	M0_SA_DQ19	J15	VDDC	L5	M0_SA_CA2	M18	M0_SB_CS0_n
H3	M0_SA_DQ16	J16	VSS	L6	M0_SA_CA1	M19	VSS
H4	NC	J17	VDDQ	L7	VDDQ	M20	NC
H5	VSS	J18	NC	L8	VSS	M21	M0_SB_DQ23
H6	NC	J19	M0_SB_CA5	L9	VDDC	M22	M0_SB_DQ20
H7	VSS	J20	NC	L10	VSS	M23	M0_SB_DQS6_t
H8	VDDQ	J21	M0_SB_DQ16	L11	VDDC	N1	M0_SA_DQS1_t
H9	VSS	J22	M0_SB_DQ19	L12	VSS	N2	M0_SA_DQ11
H10	VDDC	J23	M0_SA_DQS6_t	L13	VDDC	N3	M0_SA_DQ8
H11	VSS	K1	M0_SB_DQS1_t	L14	VSS	N4	M0_SA_CS3_n
H12	VDDC	K2	M0_SA_DQ12	L15	VDDC	N5	" M0_SA_CS2_n"
H13	VSS	K3	M0_SA_DQ15	L16	VSS	N6	M0_SA_CS1_n
H14	NC	K4	NC	L17	VDDQ	N7	VDDQ
H15	VSS	K5	VSS	L18	NC	N8	VSS
H16	VDDC	K6	M0_SA_CA6	L19	NC	N9	VDDA
H17	VSS	K7	VSS	L20	NC	N10	VSS
H18	M0_SB_CA6	K8	VDDQ	L21	VSS	N11	VDDA
H19	VSS	K9	VSS	L22	VDDQ	N12	VSS

Table 47 — Reference #3 DDR5 Use Cases Pin List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
N13	VDDC	R3	M0_SA_DQ7	T16	VDDHA	V6	VSS
N14	VSS	R4	NC	T17	NC	V7	VSS
N15	VDDC	R5	TRST_n	T18	MSCL	V8	VDDA
N16	VSS	R6	VSS	T19	NC	V9	VSS
N17	VDDQ	R7	VDDA	T20	VDD18	V10	VDDA
N18	M0_SB_CS1_n	R8	VSS	T21	VSS	V11	VSS
N19	" M0_SB_CS2_n"	R9	VDDHA	T22	VDDQ	V12	VDDA
N20	M0_SB_CS3_n	R10	VSS	T23	VSS	V13	VSS
N21	M0_SB_DQ22	R11	VDDHA	U1	M0_SA_DQS0_c	V14	VDDA
N22	M0_SB_DQ21	R12	VSS	U2	M0_SA_DQ2	V15	VSS
N23	M0_SB_DQS6_c	R13	VDDHA	U3	M0_SA_DQ1	V16	VDDA
P1	M0_SB_DQS0_c	R14	VSS	U4	TDO	V17	VSS
P2	M0_SA_DQ5	R15	VDDHA	U5	TCK	V18	VDDA
P3	M0_SA_DQ6	R16	VSS	U6	PGOOD / RESET_n	V19	VSS
P4	VSS	R17	MSDA	U7	VDD18	V20	VSS
P5	NC	R18	HSDA	U8	VSS	V21	M0_SB_DQ30
P6	NC	R19	HSCL	U9	VDDHA	V22	M0_SB_DQ29
P7	VSS	R20	VSS	U10	VSS	V23	M0_SB_DQS7_c
P8	VDDA	R21	M0_SB_DQ25	U11	VDDA	W1	VSS
P9	VSS	R22	M0_SB_DQ26	U12	VSS	W2	VSS
P10	VDDA	R23	M0_SA_DQS7_c	U13	VDDA	W3	VSS
P11	VSS	T1	VSS	U14	VSS	W4	VSS
P12	VDDC	T2	VDDQ	U15	VDDA	W5	PETX0_n
P13	VSS	T3	VSS	U16	VSS	W6	VSS
P14	VDDC	T4	TMS	U17	VDDA	W7	PETX1_n
P15	VSS	T5	TDI	U18	NC	W8	VSS
P16	VDDC	T6	VDD18	U19	NC	W9	PETX2_n
P17	VSS	T7	VSS	U20	VDD18	W10	VSS
P18	VDD10	T8	VDDHA	U21	M0_SB_DQ31	W11	PETX3_n
P19	NC	T9	VSS	U22	M0_SB_DQ28	W12	VSS
P20	VDD18	T10	VDDHA	U23	M0_SB_DQS7_t	W13	PETX4_n
P21	M0_SB_DQ24	T11	VSS	V1	M0_SA_DQS0_t	W14	VSS
P22	M0_SB_DQ27	T12	VDDHA	V2	M0_SA_DQ3	W15	PETX5_n
P23	M0_SA_DQS7_t	T13	VSS	V3	M0_SA_DQ0	W16	VSS
R1	M0_SB_DQS0_t	T14	VDDHA	V4	VSS	W17	PETX6_n
R2	M0_SA_DQ4	T15	VSS	V5	VSS	W18	VSS

Table 47 — Reference #3 DDR5 Use Cases Pin List (cont'd)

No.	Name	No.	Name	No.	Name
W19	PETX7_n	AA9	VSS	AB22	NC
W20	VSS	AA10	VSS	AB23	NC
W21	NC	AA11	VSS	AC1	VSS
W22	NC	AA12	VSS	AC2	VSS
W23	VSS	AA13	VSS	AC3	VSS
Y1	REFCLK_p	AA14	VSS	AC4	PERX0_p
Y2	REFCLK_n	AA15	VSS	AC5	VSS
Y3	VSS	AA16	VSS	AC6	PERX1_p
Y4	VSS	AA17	VSS	AC7	VSS
Y5	PETX0_p	AA18	VSS	AC8	PERX2_p
Y6	VSS	AA19	VSS	AC9	VSS
Y7	PETX1_p	AA20	VSS	AC10	PERX3_p
Y8	VSS	AA21	SIO0	AC11	VSS
Y9	PETX2_p	AA22	RXD	AC12	PERX4_p
Y10	VSS	AA23	TXD	AC13	VSS
Y11	PETX3_p	AB1	PECLK_t	AC14	PERX5_p
Y12	VSS	AB2	PECLK_n	AC15	VSS
Y13	PETX4_p	AB3	VSS	AC16	PERX6_p
Y14	VSS	AB4	PERX0_n	AC17	VSS
Y15	PETX5_p	AB5	VSS	AC18	PERX7_p
Y16	VSS	AB6	PERX1_n	AC19	VSS
Y17	PETX6_p	AB7	VSS	AC20	GPIO1
Y18	VSS	AB8	PERX2_n	AC21	GPIO0
Y19	PETX7_p	AB9	VSS	AC22	PERST_n
Y20	VSS	AB10	PERX3_n	AC23	VSS
Y21	SCS_n	AB11	VSS		
Y22	SIO3	AB12	PERX4_n		
Y23	SCLK	AB13	VSS		
AA1	VSS	AB14	PERX5_n		
AA2	VSS	AB15	VSS		
AA3	VSS	AB16	PERX6_n		
AA4	VSS	AB17	VSS		
AA5	VSS	AB18	PERX7_n		
AA6	VSS	AB19	VSS		
AA7	VSS	AB20	SIO2		
AA8	VSS	AB21	SIO1		

11.3 Reference #4 DDR4 Use Case Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	VSS	M0_DQS3_1	M0_DQS3_c	VSS	M0_DQS13_1	M0_DQS13_c	M0_DQS8_1	M0_DQS8_c	VSS	M0_DQS18_1	M0_DQS18_c	VSS	M0_DQS9_1	M0_DQS9_c	VSS	M0_DQS19_1	M0_DQS19_c	M0_DQS4_1	M0_DQS4_c	VSS	M0_DQS14_1	M0_DQS14_c	VSS
B	VDDQ	M0_DQ27	M0_DQ26	VDDQ	M0_DQ28	M0_DQ29	M0_CB3	M0_CB2	VDDQ	M0_CB4	M0_CB5	VDDQ	NC	NC	VDDQ	NC	NC	M0_DQ35	M0_DQ34	VDDQ	M0_DQ36	M0_DQ37	VDDQ
C	VSS	M0_DQ24	M0_DQ25	VSS	M0_DQ31	M0_DQ30	M0_CB0	M0_CB1	VSS	M0_CB7	M0_CB6	VSS	NC	NC	VSS	NC	NC	M0_DQ32	M0_DQ33	VSS	M0_DQ39	M0_DQ38	VSS
D	M0_DQS12_c	M0_DQ21	M0_DQ22	VSS	M0_CKB_c	VSS	M0_CKA_c	VSS	M0_ZQCAL	VSS	NC	VSS	BOOTSEL1	VSS	BOOTSEL0	VSS	M0_CKC_c	VSS	M0_CKD_c	VSS	M0_DQ40	M0_DQ43	M0_DQS5_1
E	M0_DQS12_t	M0_DQ20	M0_DQ23	VSS	M0_CKB_t	VSS	M0_CKA_t	VSS	NC	VSS	M0_RESET_n	VSS	NC	VDD18	NC	VSS	M0_CKC_t	VSS	M0_CKD_t	VSS	M0_DQ41	M0_DQ42	M0_DQS5_c
F	VSS	VDDQ	VSS	M0_A4	VSS	M0_ALERT_n	VSS	VDDQ	VSS	VDDQ	VSS	VSS	VSS	VDDQ	VSS	VDDQ	VSS	M0_CS2_n	VSS	M0_A0	VSS	VDDQ	VSS
G	M0_DQS2_c	M0_DQ18	M0_DQ17	M0_A1	M0_A3	M0_A6	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	NC	VSS	VDDQ	VSS	VDDQ	M0_WEn/M0_A14	M0_AP/M0_A10	M0_A13	M0_DQ47	M0_DQ44	M0_DQS15_t
H	M0_DQS2_t	M0_DQ19	M0_DQ16	M0_A7	VSS	M0_BC_n/M0_A12	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	NC	VSS	VDDQ	VSS	M0_CID2	VSS	M0_CID0	M0_DQ45	M0_DQ46	M0_DQS15_c
J	M0_DQS11_c	M0_DQ13	M0_DQ14	M0_BA1	M0_ACT_n	M0_BG0	VDDQ	VSS	VDDQ	VSS	VDD18	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	M0_CS3_n	M0_CS0_n	M0_PAR	M0_DQ48	M0_DQ51	M0_DQS6_t
K	M0_DQS11_t	M0_DQ12	M0_DQ15	M0_A2	VSS	M0_A5	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	M0_CAS_n/M0_A15	VSS	M0_BA0	M0_DQ49	M0_DQ50	M0_DQS6_c
L	VSS	VDDQ	VSS	M0_A8	M0_BG1	M0_A9	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	M0_A17	M0_CS1_n	M0_RAS_n/M0_A16	VSS	VDDQ	VSS
M	M0_DQS1_c	M0_DQ10	M0_DQ9	M0_A11	VSS	M0_CKE0	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	M0_ODT0	VSS	M0_CID1	M0_DQ55	M0_DQ52	M0_DQS16_t
N	M0_DQS1_t	M0_DQ11	M0_DQ8	M0_CKE3	M0_CKE2	M0_CKE1	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	M0_ODT1	M0_ODT2	M0_ODT3	M0_DQ56	M0_DQ53	M0_DQS16_c
P	M0_DQS10_c	M0_DQ5	M0_DQ6	VSS	NC	NC	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	NC	VDD18	M0_DQ57	M0_DQ58	M0_DQS7_t
R	M0_DQS10_t	M0_DQ4	M0_DQ7	NC	TRST_n	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	MSDA	HSDA	HSCL	VSS	M0_DQ59	M0_DQ58	M0_DQS7_c
T	VSS	VDDQ	VSS	TMS	TDI	VDD18	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	NC	MSCL	NC	VDD18	VSS	VDDQ	VSS
U	M0_DQS0_c	M0_DQ2	M0_DQ1	TDO	TCK	PGOOD / RESET_n	VDD18	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	NC	NC	VDD18	M0_DQ63	M0_DQ60	M0_DQS17_t
V	M0_DQS0_t	M0_DQ3	M0_DQ0	VSS	VSS	VSS	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VSS	M0_DQ62	M0_DQ61	M0_DQS17_c
W	VSS	VSS	VSS	VSS	PETX0_n	VSS	PETX1_n	VSS	PETX2_n	VSS	PETX3_n	VSS	PETX4_n	VSS	PETX5_n	VSS	PETX6_n	VSS	PETX7_n	VSS	NC	NC	VSS
Y	REFCLK_p	REFCLK_n	VSS	VSS	PETX0_p	VSS	PETX1_p	VSS	PETX2_p	VSS	PETX3_p	VSS	PETX4_p	VSS	PETX5_p	VSS	PETX6_p	VSS	PETX7_p	VSS	SCS_n	SIO3	SCLK
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SIO0	RXD	TXD
AB	PECLK_t	PECLK_n	VSS	PERX0_n	VSS	PERX1_n	VSS	PERX2_n	VSS	PERX3_n	VSS	PERX4_n	VSS	PERX5_n	VSS	PERX6_n	VSS	PERX7_n	VSS	SIO2	SIO1	NC	NC
AC	VSS	VSS	VSS	PERX0_p	VSS	PERX1_p	VSS	PERX2_p	VSS	PERX3_p	VSS	PERX4_p	VSS	PERX5_p	VSS	PERX6_p	VSS	PERX7_p	VSS	GPIO1	GPIO0	PERST_n	VSS

Figure 14 — Reference #4 DDR4 Use Case Ball Map

11.3 Reference #4 DDR4 Use Case Ball Map (cont'd)

Table 48 — Reference #4 DDR4 Use Case Pin List

No.	Name	No.	Name	No.	Name	No.	Name
A1	VSS	B14	NC	D4	VSS	E17	M0_CKC_t
A2	M0_DQS3_t	B15	VDDQ	D5	M0_CKB_c	E18	VSS
A3	M0_DQS3_c	B16	NC	D6	VSS	E19	M0_CKD_t
A4	VSS	B17	NC	D7	M0_CKA_c	E20	VSS
A5	M0_DQS13_t	B18	M0_DQ35	D8	VSS	E21	M0_DQ41
A6	M0_DQS13_c	B19	M0_DQ34	D9	M0_ZQCAL	E22	M0_DQ42
A7	M0_DQS8_t	B20	VDDQ	D10	VSS	E23	M0_DQS5_c
A8	M0_DQS8_c	B21	M0_DQ36	D11	NC	F1	VSS
A9	VSS	B22	M0_DQ37	D12	VSS	F2	VDDQ
A10	M0_DQS18_t	B23	VDDQ	D13	BOOTSEL1	F3	VSS
A11	M0_DQS18_c	C1	VSS	D14	VSS	F4	M0_A4
A12	VSS	C2	M0_DQ24	D15	BOOTSEL0	F5	VSS
A13	M0_DQS9_t	C3	M0_DQ25	D16	VSS	F6	M0_ALERT_n
A14	M0_DQS9_c	C4	VSS	D17	M0_CKC_c	F7	VSS
A15	VSS	C5	M0_DQ31	D18	VSS	F8	VDDQ
A16	M0_DQS19_t	C6	M0_DQ30	D19	M0_CKD_c	F9	VSS
A17	M0_DQS19_c	C7	M0_CB0	D20	VSS	F10	VDDQ
A18	M0_DQS4_t	C8	M0_CB1	D21	M0_DQ40	F11	VSS
A19	M0_DQS4_c	C9	VSS	D22	M0_DQ43	F12	VSS
A20	VSS	C10	M0_CB7	D23	M0_DQS5_t	F13	VSS
A21	M0_DQS14_t	C11	M0_CB6	E1	M0_DQS12_t	F14	VDDQ
A22	M0_DQS14_c	C12	VSS	E2	M0_DQ20	F15	VSS
A23	VSS	C13	NC	E3	M0_DQ23	F16	VDDQ
B1	VDDQ	C14	NC	E4	VSS	F17	VSS
B2	M0_DQ27	C15	VSS	E5	M0_CKB_t	F18	M0_CS2_n
B3	M0_DQ26	C16	NC	E6	VSS	F19	VSS
B4	VDDQ	C17	NC	E7	M0_CKA_t	F20	M0_A0
B5	M0_DQ28	C18	M0_DQ32	E8	VSS	F21	VSS
B6	M0_DQ29	C19	M0_DQ33	E9	NC	F22	VDDQ
B7	M0_CB3	C20	VSS	E10	VSS	F23	VSS
B8	M0_CB2	C21	M0_DQ39	E11	M0_RESET_n	G1	M0_DQS2_c
B9	VDDQ	C22	M0_DQ38	E12	VSS	G2	M0_DQ18
B10	M0_CB4	C23	VSS	E13	NC	G3	M0_DQ17
B11	M0_CB5	D1	M0_DQS12_c	E14	VDD18	G4	M0_A1
B12	VDDQ	D2	M0_DQ21	E15	NC	G5	M0_A3
B13	NC	D3	M0_DQ22	E16	VSS	G6	M0_A6

Table 48 — Reference #4 DDR4 Use Case Pin List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
G7	VDDQ	H20	M0_CID0	K10	VDDC	L23	VSS
G8	VSS	H21	M0_DQ46	K11	VSS	M1	M0_DQS1_c
G9	VDDQ	H22	M0_DQ45	K12	VDDC	M2	M0_DQ10
G10	VSS	H23	M0_DQS15_c	K13	VSS	M3	M0_DQ9
G11	VDDQ	J1	M0_DQS11_c	K14	VDDC	M4	M0_A11
G12	VSS	J2	M0_DQ13	K15	VSS	M5	VSS
G13	NC	J3	M0_DQ14	K16	VDDC	M6	M0_CKE0
G14	VSS	J4	M0_BA1	K17	VSS	M7	VSS
G15	VDDQ	J5	M0_ACT_n	K18	M0_CAS_n/M0_A15	M8	VDDQ
G16	VSS	J6	M0_BG0	K19	VSS	M9	VSS
G17	VDDQ	J7	VDDQ	K20	M0_BA0	M10	VDDA
G18	M0_WE_n/M0_A14	J8	VSS	K21	M0_DQ49	M11	VSS
G19	M0_AP/M0_A10	J9	VDDC	K22	M0_DQ50	M12	VDDC
G20	M0_A13	J10	VSS	K23	M0_DQS6_c	M13	VSS
G21	M0_DQ47	J11	VDD18	L1	VSS	M14	VDDC
G22	M0_DQ44	J12	VSS	L2	VDDQ	M15	VSS
G23	M0_DQS15_t	J13	VDDC	L3	VSS	M16	VDDA
H1	M0_DQS2_t	J14	VSS	L4	M0_A8	M17	VSS
H2	M0_DQ19	J15	VDDC	L5	M0_BG1	M18	M0_ODT0
H3	M0_DQ16	J16	VSS	L6	M0_A9	M19	VSS
H4	M0_A7	J17	VDDQ	L7	VDDQ	M20	M0_CID1
H5	VSS	J18	M0_CS3_n	L8	VSS	M21	M0_DQ55
H6	M0_BC_n/M0_A12	J19	M0_CS0_n	L9	VDDC	M22	M0_DQ52
H7	VSS	J20	M0_PAR	L10	VSS	M23	M0_DQS16_t
H8	VDDQ	J21	M0_DQ48	L11	VDDC	N1	M0_DQS1_t
H9	VSS	J22	M0_DQ51	L12	VSS	N2	M0_DQ11
H10	VDDC	J23	M0_DQS6_t	L13	VDDC	N3	M0_DQ8
H11	VSS	K1	M0_DQS11_t	L14	VSS	N4	M0_CKE3
H12	VDDC	K2	M0_DQ12	L15	VDDC	N5	M0_CKE2
H13	VSS	K3	M0_DQ15	L16	VSS	N6	M0_CKE1
H14	NC	K4	M0_A2	L17	VDDQ	N7	VDDQ
H15	VSS	K5	VSS	L18	M0_A17	N8	VSS
H16	VDDC	K6	M0_A5	L19	M0_CS1_n	N9	VDDA
H17	VSS	K7	VSS	L20	M0_RAS_n/M0_A16	N10	VSS
H18	M0_CID2	K8	VDDQ	L21	VSS	N11	VDDA
H19	VSS	K9	VSS	L22	VDDQ	N12	VSS

Table 48 — Reference #4 DDR4 Use Case Pin List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
N13	VDDC	R3	M0_DQ7	T16	VDDHA	V6	VSS
N14	VSS	R4	NC	T17	NC	V7	VSS
N15	VDDC	R5	TRST_n	T18	MSCL	V8	VDDA
N16	VSS	R6	VSS	T19	NC	V9	VSS
N17	VDDQ	R7	VDDA	T20	VDD18	V10	VDDA
N18	M0_ODT1	R8	VSS	T21	VSS	V11	VSS
N19	M0_ODT2	R9	VDDHA	T22	VDDQ	V12	VDDA
N20	M0_ODT3	R10	VSS	T23	VSS	V13	VSS
N21	M0_DQ54	R11	VDDHA	U1	M0_DQS0_c	V14	VDDA
N22	M0_DQ53	R12	VSS	U2	M0_DQ2	V15	VSS
N23	M0_DQS16_c	R13	VDDHA	U3	M0_DQ1	V16	VDDA
P1	M0_DQS10_c	R14	VSS	U4	TDO	V17	VSS
P2	M0_DQ5	R15	VDDHA	U5	TCK	V18	VDDA
P3	M0_DQ6	R16	VSS	U6	PGOOD / RESET_n	V19	VSS
P4	VSS	R17	MSDA	U7	VDD18	V20	VSS
P5	NC	R18	HSDA	U8	VSS	V21	M0_DQ62
P6	NC	R19	HSCL	U9	VDDHA	V22	M0_DQ61
P7	VSS	R20	VSS	U10	VSS	V23	M0_DQS17_c
P8	VDDA	R21	M0_DQ57	U11	VDDA	W1	VSS
P9	VSS	R22	M0_DQ58	U12	VSS	W2	VSS
P10	VDDA	R23	M0_DQS7_c	U13	VDDA	W3	VSS
P11	VSS	T1	VSS	U14	VSS	W4	VSS
P12	VDDC	T2	VDDQ	U15	VDDA	W5	PETX0_n
P13	VSS	T3	VSS	U16	VSS	W6	VSS
P14	VDDC	T4	TMS	U17	VDDA	W7	PETX1_n
P15	VSS	T5	TDI	U18	NC	W8	VSS
P16	VDDC	T6	VDD18	U19	NC	W9	PETX2_n
P17	VSS	T7	VSS	U20	VDD18	W10	VSS
P18	VDD10	T8	VDDHA	U21	M0_DQ63	W11	PETX3_n
P19	NC	T9	VSS	U22	M0_DQ60	W12	VSS
P20	VDD18	T10	VDDHA	U23	M0_DQS17_t	W13	PETX4_n
P21	M0_DQ56	T11	VSS	V1	M0_DQS0_t	W14	VSS
P22	M0_DQ59	T12	VDDHA	V2	M0_DQ3	W15	PETX5_n
P23	M0_DQS7_t	T13	VSS	V3	M0_DQ0	W16	VSS
R1	M0_DQS10_t	T14	VDDHA	V4	VSS	W17	PETX6_n
R2	M0_DQ4	T15	VSS	V5	VSS	W18	VSS

Table 48 — Reference #4 DDR4 Use Case Pin List (cont'd)

No.	Name	No.	Name	No.	Name
W19	PETX7_n	AA9	VSS	AB22	NC
W20	VSS	AA10	VSS	AB23	NC
W21	NC	AA11	VSS	AC1	VSS
W22	NC	AA12	VSS	AC2	VSS
W23	VSS	AA13	VSS	AC3	VSS
Y1	REFCLK_p	AA14	VSS	AC4	PERX0_p
Y2	REFCLK_n	AA15	VSS	AC5	VSS
Y3	VSS	AA16	VSS	AC6	PERX1_p
Y4	VSS	AA17	VSS	AC7	VSS
Y5	PETX0_p	AA18	VSS	AC8	PERX2_p
Y6	VSS	AA19	VSS	AC9	VSS
Y7	PETX1_p	AA20	VSS	AC10	PERX3_p
Y8	VSS	AA21	SIO0	AC11	VSS
Y9	PETX2_p	AA22	RXD	AC12	PERX4_p
Y10	VSS	AA23	TXD	AC13	VSS
Y11	PETX3_p	AB1	PECLK_t	AC14	PERX5_p
Y12	VSS	AB2	PECLK_n	AC15	VSS
Y13	PETX4_p	AB3	VSS	AC16	PERX6_p
Y14	VSS	AB4	PERX0_n	AC17	VSS
Y15	PETX5_p	AB5	VSS	AC18	PERX7_p
Y16	VSS	AB6	PERX1_n	AC19	VSS
Y17	PETX6_p	AB7	VSS	AC20	GPIO1
Y18	VSS	AB8	PERX2_n	AC21	GPIO0
Y19	PETX7_p	AB9	VSS	AC22	PERST_n
Y20	VSS	AB10	PERX3_n	AC23	VSS
Y21	SCS_n	AB11	VSS		
Y22	SIO3	AB12	PERX4_n		
Y23	SCLK	AB13	VSS		
AA1	VSS	AB14	PERX5_n		
AA2	VSS	AB15	VSS		
AA3	VSS	AB16	PERX6_n		
AA4	VSS	AB17	VSS		
AA5	VSS	AB18	PERX7_n		
AA6	VSS	AB19	VSS		
AA7	VSS	AB20	SIO2		
AA8	VSS	AB21	SIO1		

12 Appendix C

This appendix contains example ball maps for informational purposes.

12.1 Ball Map Use Cases

The x16 CMC01 Standard Package is a 25x25mm² 0.8 mm pitch 31x31 ball array

The DDR4 and DDR5 are the two use cases for the x16 CMC01 Standard Package; there is a separate ball map for each use case.

12.2 Reference #5 DDR5 Use Case Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31					
A	VSS	M0_SA_DQ55_1	VSS	VSS	M0_SB_DQ55_1	M0_SB_DQ14	VSS	M0_SB_DQ18	M0_SA_DQ56_1	M0_SB_DQ22	M0_SB_DQ26	M0_SA_DQ57_1	M0_SB_DQ30	VSS	M1_SB_DQ30	M1_SB_DQ57_1	M1_SA_DQ57_1	M1_SB_DQ26	M1_SB_DQ22	M1_SB_DQ56_1	M1_SA_DQ56_1	M1_SB_DQ18	VSS	M1_SB_DQ14	M1_SB_DQ55_1	VSS	VSS	M1_SA_DQ55_1	VSS							
B	M0_SB_DQ30	M0_SA_DQ55_1	M0_SB_DQ29	VDDQ	M0_SB_DQ25_1	M0_SB_DQ13	VSS	M0_SB_DQ19	M0_SA_DQ34_1	M0_SB_DQ26_1	M0_SB_DQ21	M0_SB_DQ27	M0_SA_DQ57_1	M0_SB_DQ29	VSS	M1_SB_DQ29	M1_SB_DQ57_1	M1_SA_DQ57_1	M1_SB_DQ27	M1_SB_DQ23	M1_SB_DQ56_1	M1_SA_DQ56_1	M1_SB_DQ19	VSS	M1_SB_DQ13	M1_SB_DQ25_1	VDDQ	M1_SB_DQ29	M1_SA_DQ55_1	M1_SB_DQ30						
C	M0_SB_DQ11	VSS	M0_SB_DQ8	VSS	VDDQ	M0_SB_DQ12	VSS	VSS	M0_SB_DQ17	VSS	M0_SB_DQ20	VSS	M0_SB_DQ25	VSS	M1_SB_DQ28	VSS	M1_SB_DQ25	VSS	M1_SB_DQ20	VSS	M1_SB_DQ17	VSS	VSS	M1_SB_DQ12	VDDQ	VSS	M1_SB_DQ8	VSS	M1_SB_DQ11							
D	M0_SB_DQ6	M0_SB_DQ5	M0_SB_DQ4	VDDQ	M0_SB_DQ15	VDDQ	VSS	M0_SB_DQ16	VDDQ	M0_SB_DQ23	VDDQ	M0_SB_DQ24	VDDQ	M0_SB_DQ31	VDDQ	VSS	VDDQ	M1_SB_DQ33	VDDQ	M1_SB_DQ24	VDDQ	M1_SB_DQ23	VDDQ	M1_SB_DQ16	VSS	VDDQ	M1_SB_DQ15	VDDQ	M1_SB_DQ4	M1_SB_DQ6						
E	M0_SB_DQ54_1	M0_SB_DQ54_1	VSS	M0_SB_DQ7	M0_SB_C_S2_n	VSS	M0_SB_C_S1_n	M0_SB_C_S0_n	M0_RESE_T_n	M0_ZOC_AL	O_NOT_CONNECT	O_NOT_CONNECT	TEN	BOOTSEL_0	BOOTSEL_1	RSTSEL0	RSTSEL1	THERM_PADB	PWR_EN	RSVD_0_O_NOT_CONNECT	RSVD_1_O_NOT_CONNECT	M1_ZOC_AL	M1_RESE_T_n	M1_SB_C_S0_n	M1_SB_C_S1_n	VSS	M1_SB_C_S2_n	M1_SB_DQ7	VSS	M1_SB_DQ54_1						
F	M0_SA_DQ54_1	M0_SA_DQ54_1	M0_SB_DQ1	VDDQ	M0_SB_C_A3	VSS	M0_SB_C_A1	M0_SB_C_S3_n	M0_EVE_NT_n	VSS	M0_DIB_DQ	M0_DIB_DQ5	VSS	SAVE_N	CLKSEL	VSS	PWRDIS	THERM_PADE	VSS	M1_DIB_DQ5	M1_DIB_DQ	VSS	M1_EVE_NT_n	M1_SB_C_S3_n	VSS	M1_SB_C_A1	M1_SB_C_A3	VDDQ	M1_SB_DQ1	M1_SA_DQ54_1						
G	M0_SB_DQ2	M0_SB_DQ3	VSS	M0_SB_DQ0	M0_SB_C_A9	VSS	M0_SB_C_A7/M0_5_B_DPAR	M0_SB_C_A5	M0_Vref_CA	LED1	LED2	RCRVY	PCAMP	FAIL_N	VDD18	GPIO7	VDD18	GPIO6	PGOOD_DDR/PCAMP	GPIO5	GPIO4	GPIO3	M1_Vref_CA	M1_SB_C_A5	M1_SB_C_A7/M1_5_B_DPAR	VSS	M1_SB_C_A9	M1_SB_DQ0	VSS	M1_SB_DQ3	M1_SB_DQ2					
H	M0_SB_C_B6	M0_SB_C_B5	M0_SB_C_B4	VDDQ	M0_SB_C_A13	M0_SB_C_A11	VSS	M0_SB_C_A0	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDD18	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	M1_SB_C_A0	VSS	M1_SB_C_A11	M1_SB_C_A13	VDDQ	M1_SB_C_B4	M1_SB_C_B5	M1_SB_C_B6			
J	M0_SB_DQ39_1	M0_SB_DQ39_1	VSS	M0_SB_C_B7	VSS	VSS	M0_SB_C_A4	M0_SB_C_A2	LED0	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	GPIO2	M1_SB_C_A2	M1_SB_C_A4	VSS	VSS	M1_SB_C_B7	VSS	M1_SB_DQ39_1						
K	M0_SA_DQ59_1	M0_SA_DQ59_1	M0_SB_C_B1	VDDQ	M0_SA_C_KB_c	VSS	M0_SA_C_KB_1	VSS	M0_SB_C_A6	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDD18	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	M1_SB_C_A6	VSS	M1_SA_C_KB_1	M1_SA_C_KB_c	VDDQ	M1_SB_C_B1	M1_SA_DQ59_1			
L	M0_SB_C_B2	M0_SB_C_B3	VSS	M0_SB_C_B0	VSS	VSS	M0_SB_C_A8	M0_SB_C_A10	DEBUG3	VSS	VDDQ	VSS	VDDQ	VSS	VSS	VSS	VDDC	VSS	VDDQ	VSS	VDDQ	VSS	GPIO1	M1_SB_C_A10	M1_SB_C_A8	VSS	VSS	M1_SB_C_B0	VSS	M1_SB_C_B2						
M	M0_SA_C_B6	M0_SA_C_B5	M0_SA_C_B4	VDDQ	M0_SB_C_KB_c	VSS	M0_SB_C_KB_1	VSS	M0_SB_C_A12	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VDD18	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	M1_SB_C_A12	VSS	M1_SB_C_KB_c	M1_SB_C_KB_1	VDDQ	M1_SA_C_B4	M1_SA_C_B5	M1_SA_C_B6				
N	M0_SB_DQ58_1	M0_SB_DQ58_1	VSS	M0_SB_C_B7	VSS	VSS	DDR0_A0_2H_NC_P_ARB	DDR0_C5_2H_NC_P_ARB	DEBUG2	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	GPIO0	DDR1_C5_2H_NC_P_ARB	DDR1_A4_2H_NC_P_ARB	VSS	VSS	M1_SB_C_B7	VSS	M1_SB_DQ58_1						
P	M0_SA_DQ58_1	M0_SA_DQ58_1	M0_SA_C_B1	VDDQ	VSS	VSS	DDR0_A4_2H_NC_P_ARB	DDR0_A1_2H_NC_P_ARB	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	M1_ALER_T_n	DDR1_A4_2H_NC_P_ARB	VSS	VSS	VDDQ	M1_SA_C_B1	M1_SA_DQ58_1						
R	M0_SA_C_B7	M0_SA_C_B3	VSS	M0_SA_C_B0	VSS	M0_SA_C_KA_c	M0_SA_C_KA_1	VSS	M0_SA_C_A12	DEBUG1	VSS	VDDQ	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDA	VSS	VDDQ	VSS	EVENT_N	M1_SA_C_A12	VSS	M1_SA_C_KA_1	M1_SA_C_KA_c	M1_SA_C_B0	VSS	M1_SA_C_B7					
T	M0_SA_DQ30	M0_SA_DQ29	M0_SA_DQ28	VDDQ	VSS	VSS	M0_SA_C_A10	M0_SA_C_A8	VSS	VDDQ	VSS	VDDC	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	VDDQ	VSS	M1_SA_C_A8	M1_SA_C_A10	VSS	VSS	VDDQ	M1_SA_DQ28	M1_SA_DQ29	M1_SA_DQ30			
U	M0_SB_DQ53_1	M0_SB_DQ53_1	VSS	M0_SA_DQ31	VSS	VSS	M0_SB_C_KA_c	M0_SB_C_KA_1	VSS	DEBUG0	VSS	VDDQ	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	M_SCAN_PCAP_5_EL	M1_SA_C_A6	VSS	M1_SB_C_KA_1	M1_SB_C_KA_c	VSS	M1_SB_DQ53_1						
V	M0_SA_DQ53_1	M0_SA_DQ53_1	M0_SA_DQ25	VDDQ	VSS	VSS	M0_SA_C_A4	M0_SA_C_A2	VSS	RSVD_0_O_NOT_CONNECT	RSVD_1_O_NOT_CONNECT	VDDC	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDD010	VSS	MSDA	HSCL	M1_SA_C_A2	M1_SA_C_A4	VSS	VSS	VDDQ	M1_SA_DQ25	M1_SA_DQ53_1						
W	M0_SA_DQ26	M0_SA_DQ27	VSS	M0_SA_DQ24	M0_SA_C_A13	VSS	M0_SA_C_A11	M0_SA_C_A0	VDD18	VSS	VDDA	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDD18	MSCL	HSDA	M1_SA_C_A0	VSS	M1_SA_C_A11	M1_SA_C_A13	M1_SA_DQ24	VSS	M1_SA_DQ26						
Y	M0_SA_DQ23	M0_SA_DQ21	M0_SA_DQ20	VDDQ	M0_SA_C_A9	VSS	M0_SA_C_A7/M0_5_A_DPAR	M0_SA_C_A5	VSS	VDD18	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDD18	VSS	M1_SA_C_A5	M1_SA_C_A7/M1_5_A_DPAR	VSS	M1_SA_C_A9	VDDQ	M1_SA_DQ20	M1_SA_DQ21	M1_SA_DQ23					
AA	M0_SB_DQ52_1	M0_SB_DQ52_1	VSS	M0_SA_DQ23	M0_SA_C_A3	VSS	M0_SA_C_A1	M0_SA_C_S3_n	VDD18	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDD18	VSS	VDD18	M1_SA_C_S3_n	VSS	M1_SA_C_A1	M1_SA_C_A3	VSS	M1_SB_DQ52_1							
AB	M0_SA_DQ52_1	M0_SA_DQ52_1	M0_SA_DQ17	VDDQ	M0_SA_C_S2_n	VSS	M0_SA_C_S1_n	M0_SA_C_S0_n	PGOOD/RESET_n	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	HS40	M1_SA_C_S0_n	M1_SA_C_S1_n	VSS	M1_SA_C_S2_n	VDDQ	M1_SA_DQ17	M1_SA_DQ52_1
AC	M0_SA_DQ18	M0_SA_DQ19	VSS	M0_SA_DQ16	TRST_n	TAP_SEL	TDI	TMUXSEL_0	TMUXSEL_1	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	HS41	HS42	IDC_SCL	IDC_SDA	IDC_SRT_B	M1_SA_DQ16	VSS	M1_SA_DQ18						
AD	M0_SA_DQ14	M0_SA_DQ13	M0_SA_DQ12	VDDQ	TDO	TCK	TMS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CLKREQ_n	RWD	VDDQ	M1_SA_DQ12	M1_SA_DQ13	M1_SA_DQ14			
AE	M0_SB_DQ51_1	M0_SB_DQ51_1	VSS	M0_SA_DQ15	VSS	VSS	VSS	VSS	PETX1_n	VSS	PETX3_n	VSS	PETX5_n	VSS	PETX7_n	VSS	VSS	PETX9_n	VSS	PETX11_n	VSS	PETX13_n	VSS	PETX15_n	VSS	DUALPO_RTEN_n	TXD	VSS	M1_SB_DQ51_1							
AF	M0_SA_DQ51_1	M0_SA_DQ51_1	M0_SA_DQ9	VDDQ	VSS	REFCLK_n	VSS	PETX0_n	PETX1_p	PETX2_n	PETX3_p	PETX4_n	PETX5_p	PETX6_n	PETX7_p	VSS	PETX8_n	PETX9_p	PETX10_n	PETX11_p	PETX12_n	PETX13_p	PETX14_n	PETX15_p	VSS	PERE50	PERE51	VDDQ	M1_SA_DQ9	M1_SA_DQ51_1						
AG	M0_SA_DQ10	M0_SA_DQ11	VSS	M0_SA_DQ8	VSS	REFCLK_p	VSS	PETX0_p	PETX1_n	PETX2_p	VSS	PETX4_p	VSS	PETX6_p	VSS	VSS	PETX8_p	VSS	PETX10_p	VSS	PETX12_p	VSS	PETX14_p	VSS	VSS	PERST0_n	PERST1_n	VSS	M1_SA_DQ10	M1_SA_DQ11						
AH	M0_SA_DQ6	M0_SA_DQ5	M0_SA_DQ4	VDDQ	VSS	PECLKO_n	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD_0_O_NOT_CONNECT	RSVD_1_O_NOT_CONNECT	VDDQ	M1_SA_DQ4	M1_SA_DQ5	M1_SA_DQ6				
AJ	M0_SB_DQ50_1	M0_SB_DQ50_1	VSS	M0_SA_DQ7	VSS	PECLK1_n	VSS	VSS	PERX1_p	VSS	PERX3_p	VSS	PERX5_n	VSS	PERX7_n	VSS	VSS	PERX9_p	VSS	PERX11_p	VSS	PERX13_n	VSS	PERX15_n	VSS	SIO2	SIO3	M1_SA_DQ7	VSS	M1_SB_DQ50_1						
AK	M0_SA_DQ50_1	M0_SA_DQ50_1	M0_SA_DQ1	VDDQ	VSS	PECLK1_n	VSS	PERX0_p	PERX1_n	PERX2_p	PERX3_n	PERX4_n	PERX5_p	PERX6_n	PERX7_p	VSS	PERX8_p	PERX9_n	PERX10_p	PERX11_n	PERX12_p	PERX13_p	PERX14_n	PERX15_p	VSS	SCS_n	SIO1	VDDQ	M1_SA_DQ1	M1_SA_DQ50_1						
AL	VSS	M0_SA_DQ2	M0_SA_DQ3	VSS	PECLK1_n	VSS	PERX0_n	VSS	PERX2_n	VSS	PERX4_n	VSS	PERX6_p	VSS	VSS	VSS	PERX8_n	VSS	PERX10_n	VSS	PERX12_p	VSS	PERX14_p	VSS	VSS	SCLK	SIO0	M1_SA_DQ3	M1_SA_DQ2	VSS						

Figure 15 — Reference #5 DDR5 Use Case Ball Map

12.2 Reference #5 DDR5 Use Case Ball Map (cont'd)**Table 49 — Reference #5 DDR5 Use Case Ball Name to Number List**

No.	Name	No.	Name	No.	Name	No.	Name
A1	VSS	B6	M0_SB_DQ13	C11	M0_SB_DQ20	D16	VSS
A2	M0_SA_DQS5_t	B7	VSS	C12	VSS	D17	VDDQ
A3	VSS	B8	M0_SB_DQ19	C13	M0_SB_DQ25	D18	M1_SB_DQ31
A4	VSS	B9	M0_SA_DQS6_c	C14	VSS	D19	VDDQ
A5	M0_SB_DQS5_t	B10	M0_SB_DQS6_c	C15	M0_SB_DQ28	D20	M1_SB_DQ24
A6	M0_SB_DQ14	B11	M0_SB_DQ21	C16	VSS	D21	VDDQ
A7	VSS	B12	M0_SB_DQ27	C17	M1_SB_DQ28	D22	M1_SB_DQ23
A8	M0_SB_DQ18	B13	M0_SA_DQS7_c	C18	VSS	D23	VDDQ
A9	M0_SA_DQS6_t	B14	M0_SB_DQS7_c	C19	M1_SB_DQ25	D24	M1_SB_DQ16
A10	M0_SB_DQS6_t	B15	M0_SB_DQ29	C20	VSS	D25	VSS
A11	M0_SB_DQ22	B16	VSS	C21	M1_SB_DQ20	D26	VDDQ
A12	M0_SB_DQ26	B17	M1_SB_DQ29	C22	VSS	D27	M1_SB_DQ15
A13	M0_SA_DQS7_t	B18	M1_SB_DQS7_c	C23	M1_SB_DQ17	D28	VDDQ
A14	M0_SB_DQS7_t	B19	M1_SA_DQS7_c	C24	VSS	D29	M1_SB_DQ4
A15	M0_SB_DQ30	B20	M1_SB_DQ27	C25	VSS	D30	M1_SB_DQ5
A16	VSS	B21	M1_SB_DQ21	C26	M1_SB_DQ12	D31	M1_SB_DQ6
A17	M1_SB_DQ30	B22	M1_SB_DQS6_c	C27	VDDQ	E1	M0_SB_DQS4_t
A18	M1_SB_DQS7_t	B23	M1_SA_DQS6_c	C28	VSS	E2	M0_SB_DQS4_c
A19	M1_SA_DQS7_t	B24	M1_SB_DQ19	C29	M1_SB_DQ8	E3	VSS
A20	M1_SB_DQ26	B25	VSS	C30	VSS	E4	M0_SB_DQ7
A21	M1_SB_DQ22	B26	M1_SB_DQ13	C31	M1_SB_DQ11	E5	M0_SB_CS2_n
A22	M1_SB_DQS6_t	B27	M1_SB_DQS5_c	D1	M0_SB_DQ6	E6	VSS
A23	M1_SA_DQS6_t	B28	VDDQ	D2	M0_SB_DQ5	E7	M0_SB_CS1_n
A24	M1_SB_DQ18	B29	M1_SB_DQ9	D3	M0_SB_DQ4	E8	M0_SB_CS0_n
A25	VSS	B30	M1_SA_DQS5_c	D4	VDDQ	E9	M0_RESET_n
A26	M1_SB_DQ14	B31	M1_SB_DQ10	D5	M0_SB_DQ15	E10	M0_ZQCAL
A27	M1_SB_DQS5_t	C1	M0_SB_DQ11	D6	VDDQ	E11	RSVD_DO_NOT_CONNECT
A28	VSS	C2	VSS	D7	VSS	E12	RSVD_DO_NOT_CONNECT
A29	VSS	C3	M0_SB_DQ8	D8	M0_SB_DQ16	E13	TEN
A30	M1_SA_DQS5_t	C4	VSS	D9	VDDQ	E14	BOOTSEL0
A31	VSS	C5	VDDQ	D10	M0_SB_DQ23	E15	BOOTSEL1
B1	M0_SB_DQ10	C6	M0_SB_DQ12	D11	VDDQ	E16	RSTSEL0
B2	M0_SA_DQS5_c	C7	VSS	D12	M0_SB_DQ24	E17	RSTSEL1
B3	M0_SB_DQ9	C8	VSS	D13	VDDQ	E18	THERM_PADB
B4	VDDQ	C9	M0_SB_DQ17	D14	M0_SB_DQ31	E19	PWR_EN
B5	M0_SB_DQS5_c	C10	VSS	D15	VDDQ	E20	RSVD_DO_NOT_CONNECT

Table 49 — Reference #5 DDR5 Use Case Ball Name to Number List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
E21	RSVD_DO_NOT_CONNECT	F26	M1_SB_CA1	G31	M1_SB_DQ2	J5	VSS
E22	M1_ZQCAL	F27	M1_SB_CA3	H1	M0_SB_CB6	J6	VSS
E23	M1_RESET_n	F28	VDDQ	H2	M0_SB_CB5	J7	M0_SB_CA4
E24	M1_SB_CS0_n	F29	M1_SB_DQ1	H3	M0_SB_CB4	J8	M0_SB_CA2
E25	M1_SB_CS1_n	F30	M1_SA_DQS4_c	H4	VDDQ	J9	LED0
E26	VSS	F31	M1_SA_DQS4_t	H5	M0_SB_CA13	J10	VSS
E27	M1_SB_CS2_n	G1	M0_SB_DQ2	H6	M0_SB_CA11	J11	VDDQ
E28	M1_SB_DQ7	G2	M0_SB_DQ3	H7	VSS	J12	VSS
E29	VSS	G3	VSS	H8	M0_SB_CA0	J13	VDDQ
E30	M1_SB_DQS4_c	G4	M0_SB_DQ0	H9	VSS	J14	VSS
E31	M1_SB_DQS4_t	G5	M0_SB_CA9	H10	VDDQ	J15	VDDQ
F1	M0_SA_DQS4_t	G6	VSS	H11	VSS	J16	VSS
F2	M0_SA_DQS4_c	G7	M0_SB_CA7/M0_SB_DPAR	H12	VDDQ	J17	VDDQ
F3	M0_SB_DQ1	G8	M0_SB_CA5	H13	VSS	J18	VSS
F4	VDDQ	G9	M0_VrefCA	H14	VDDQ	J19	VDDQ
F5	M0_SB_CA3	G10	LED1	H15	VSS	J20	VSS
F6	M0_SB_CA1	G11	LED2	H16	VDD18	J21	VDDQ
F7	VSS	G12	RCVRY	H17	VSS	J22	VSS
F8	M0_SB_CS3_n	G13	PCAMP	H18	VDDQ	J23	GPIO2
F9	M0_EVENT_n	G14	FAIL_N	H19	VSS	J24	M1_SB_CA2
F10	VSS	G15	VDD18	H20	VDDQ	J25	M1_SB_CA4
F11	M0_DLBQDQ	G16	GPIO7	H21	VSS	J26	VSS
F12	M0_DLBQDQS	G17	VDD18	H22	VDDQ	J27	VSS
F13	VSS	G18	GPIO6	H23	VSS	J28	M1_SB_CB7
F14	SAVE_N	G19	PGOOD_DDR / PCAMP	H24	M1_SB_CA0	J29	VSS
F15	CLKSEL	G20	GPIO5	H25	VSS	J30	M1_SB_DQS9_c
F16	VSS	G21	GPIO4	H26	M1_SB_CA11	J31	M1_SB_DQS9_t
F17	PWRDIS	G22	GPIO3	H27	M1_SB_CA13	K1	M0_SA_DQS9_t
F18	THERM_PADE	G23	M1_VrefCA	H28	VDDQ	K2	M0_SA_DQS9_c
F19	VSS	G24	M1_SB_CA5	H29	M1_SB_CB4	K3	M0_SB_CB1
F20	M1_DLBQDQS	G25	M1_SB_CA7/M1_SB_DPAR	H30	M1_SB_CB5	K4	VDDQ
F21	M1_DLBQDQ	G26	VSS	H31	M1_SB_CB6	K5	M0_SA_CKB_c
F22	VSS	G27	M1_SB_CA9	J1	M0_SB_DQS9_t	K6	M0_SA_CKB_t
F23	M1_EVENT_n	G28	M1_SB_DQ0	J2	M0_SB_DQS9_c	K7	VSS
F24	M1_SB_CS3_n	G29	VSS	J3	VSS	K8	M0_SB_CA6
F25	VSS	G30	M1_SB_DQ3	J4	M0_SB_CB7	K9	VSS

Table 49 — Reference #5 DDR5 Use Case Ball Name to Number List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
K10	VDDQ	L15	VSS	M20	VDDC	N25	DDR1_A0_NC_CA1B
K11	VSS	L16	VSS	M21	VSS	N26	VSS
K12	VDDQ	L17	VDDC	M22	VDDQ	N27	VSS
K13	VSS	L18	VSS	M23	VSS	N28	M1_SA_CB7
K14	VDDQ	L19	VDDQ	M24	M1_SB_CA12	N29	VSS
K15	VSS	L20	VSS	M25	VSS	N30	M1_SB_DQS8_c
K16	VDD18	L21	VDDQ	M26	M1_SB_CKB_c	N31	M1_SB_DQS8_t
K17	VSS	L22	VSS	M27	M1_SB_CKB_t	P1	M0_SA_DQS8_t
K18	VDDQ	L23	GPIO1	M28	VDDQ	P2	M0_SA_DQS8_c
K19	VSS	L24	M1_SB_CA10	M29	M1_SA_CB4	P3	M0_SA_CB1
K20	VDDQ	L25	M1_SB_CA8	M30	M1_SA_CB5	P4	VDDQ
K21	VSS	L26	VSS	M31	M1_SA_CB6	P5	VSS
K22	VDDQ	L27	VSS	N1	M0_SB_DQS8_t	P6	VSS
K23	VSS	L28	M1_SB_CB0	N2	M0_SB_DQS8_c	P7	DDR0_A4_NC_NC
K24	M1_SB_CA6	L29	VSS	N3	VSS	P8	M0_ALERT_n
K25	VSS	L30	M1_SB_CB3	N4	M0_SA_CB7	P9	VSS
K26	M1_SA_CKB_t	L31	M1_SB_CB2	N5	VSS	P10	VDDQ
K27	M1_SA_CKB_c	M1	M0_SA_CB6	N6	VSS	P11	VSS
K28	VDDQ	M2	M0_SA_CB5	N7	DDR0_A0_NC_CA1B	P12	VDDC
K29	M1_SB_CB1	M3	M0_SA_CB4	N8	DDR0_CS2N_NC_PARB	P13	VSS
K30	M1_SA_DQS9_c	M4	VDDQ	N9	DEBUG2	P14	VDDC
K31	M1_SA_DQS9_t	M5	M0_SB_CKB_c	N10	VSS	P15	VSS
L1	M0_SB_CB2	M6	M0_SB_CKB_t	N11	VDDQ	P16	VDDC
L2	M0_SB_CB3	M7	VSS	N12	VSS	P17	VSS
L3	VSS	M8	M0_SB_CA12	N13	VDDC	P18	VDDC
L4	M0_SB_CB0	M9	VSS	N14	VSS	P19	VSS
L5	VSS	M10	VDDQ	N15	VDDC	P20	VDDC
L6	VSS	M11	VSS	N16	VSS	P21	VSS
L7	M0_SB_CA8	M12	VDDC	N17	VDDC	P22	VDDQ
L8	M0_SB_CA10	M13	VSS	N18	VSS	P23	VSS
L9	DEBUG3	M14	VDDC	N19	VDDC	P24	M1_ALERT_n
L10	VSS	M15	VSS	N20	VSS	P25	DDR1_A4_NC_NC
L11	VDDQ	M16	VDD18	N21	VDDQ	P26	VSS
L12	VSS	M17	VSS	N22	VSS	P27	VSS
L13	VDDQ	M18	VDDC	N23	GPIO0	P28	VDDQ
L14	VSS	M19	VSS	N24	DDR1_CS2N_NC_PARB	P29	M1_SA_CB1

Table 49 — Reference #5 DDR5 Use Case Ball Name to Number List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
P30	M1_SA_DQS8_c	T4	VDDQ	U9	DEBUG0	V14	VDDA
P31	M1_SA_DQS8_t	T5	VSS	U10	VSS	V15	VSS
R1	M0_SA_CB2	T6	VSS	U11	VDDQ	V16	VDDC
R2	M0_SA_CB3	T7	M0_SA_CA10	U12	VSS	V17	VSS
R3	VSS	T8	M0_SA_CA8	U13	VDDA	V18	VDDC
R4	M0_SA_CB0	T9	VSS	U14	VSS	V19	VSS
R5	M0_SA_CKA_c	T10	VDDQ	U15	VDDC	V20	VDD10
R6	M0_SA_CKA_t	T11	VSS	U16	VSS	V21	VSS
R7	VSS	T12	VDDC	U17	VDDC	V22	MSDA
R8	M0_SA_CA12	T13	VSS	U18	VSS	V23	HSCL
R9	DEBUG1	T14	VDDA	U19	VDDC	V24	M1_SA_CA2
R10	VSS	T15	VSS	U20	VSS	V25	M1_SA_CA4
R11	VDDQ	T16	VDDC	U21	VDDQ	V26	VSS
R12	VSS	T17	VSS	U22	VSS	V27	VSS
R13	VDDA	T18	VDDC	U23	M_SCAN_PCAP_SEL	V28	VDDQ
R14	VSS	T19	VSS	U24	M1_SA_CA6	V29	M1_SA_DQ25
R15	VDDC	T20	VDDC	U25	VSS	V30	M1_SA_DQS3_c
R16	VSS	T21	VSS	U26	M1_SB_CKA_t	V31	M1_SA_DQS3_t
R17	VDDC	T22	VDDQ	U27	M1_SB_CKA_c	W1	M0_SA_DQ26
R18	VSS	T23	VSS	U28	M1_SA_DQ31	W2	M0_SA_DQ27
R19	VDDA	T24	M1_SA_CA8	U29	VSS	W3	VSS
R20	VSS	T25	M1_SA_CA10	U30	M1_SB_DQS3_c	W4	M0_SA_DQ24
R21	VDDQ	T26	VSS	U31	M1_SB_DQS3_t	W5	M0_SA_CA13
R22	VSS	T27	VSS	V1	M0_SA_DQS3_t	W6	M0_SA_CA11
R23	EVENT_N	T28	VDDQ	V2	M0_SA_DQS3_c	W7	VSS
R24	M1_SA_CA12	T29	M1_SA_DQ28	V3	M0_SA_DQ25	W8	M0_SA_CA0
R25	VSS	T30	M1_SA_DQ29	V4	VDDQ	W9	VDD18
R26	M1_SA_CKA_t	T31	M1_SA_DQ30	V5	VSS	W10	VSS
R27	M1_SA_CKA_c	U1	M0_SB_DQS3_t	V6	VSS	W11	VDDA
R28	M1_SA_CB0	U2	M0_SB_DQS3_c	V7	M0_SA_CA4	W12	VSS
R29	VSS	U3	VSS	V8	M0_SA_CA2	W13	VDDA
R30	M1_SA_CB3	U4	M0_SA_DQ31	V9	VSS	W14	VSS
R31	M1_SA_CB2	U5	M0_SB_CKA_c	V10	RSVD_DO_NOT_CONNECT	W15	VDDC
T1	M0_SA_DQ30	U6	M0_SB_CKA_t	V11	RSVD_DO_NOT_CONNECT	W16	VSS
T2	M0_SA_DQ29	U7	VSS	V12	VDDC	W17	VDDC
T3	M0_SA_DQ28	U8	M0_SA_CA6	V13	VSS	W18	VSS

Table 49 — Reference #5 DDR5 Use Case Ball Name to Number List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
W19	VDDC	Y24	M1_SA_CA5	AA29	VSS	AC3	VSS
W20	VSS	Y25	M1_SA_CA7/M1_SA_DPAR	AA30	M1_SB_DQS2_c	AC4	M0_SA_DQ16
W21	VDD18	Y26	VSS	AA31	M1_SB_DQS2_t	AC5	TRST_n
W22	MSCL	Y27	M1_SA_CA9	AB1	M0_SA_DQS2_t	AC6	TAP_SEL
W23	HSDA	Y28	VDDQ	AB2	M0_SA_DQS2_c	AC7	TDI
W24	M1_SA_CA0	Y29	M1_SA_DQ20	AB3	M0_SA_DQ17	AC8	TMUXSEL0
W25	VSS	Y30	M1_SA_DQ21	AB4	VDDQ	AC9	TMUXSEL1
W26	M1_SA_CA11	Y31	M1_SA_DQ22	AB5	M0_SA_CS2_n	AC10	VSS
W27	M1_SA_CA13	AA1	M0_SB_DQS2_t	AB6	VSS	AC11	VDDA
W28	M1_SA_DQ24	AA2	M0_SB_DQS2_c	AB7	M0_SA_CS1_n	AC12	VSS
W29	VSS	AA3	VSS	AB8	M0_SA_CS0_n	AC13	VDDA
W30	M1_SA_DQ27	AA4	M0_SA_DQ23	AB9	PGOOD / RESET_n	AC14	VSS
W31	M1_SA_DQ26	AA5	M0_SA_CA3	AB10	VDDA	AC15	VDDA
Y1	M0_SA_DQ22	AA6	M0_SA_CA1	AB11	VSS	AC16	VSS
Y2	M0_SA_DQ21	AA7	VSS	AB12	VDDA	AC17	VDDA
Y3	M0_SA_DQ20	AA8	M0_SA_CS3_n	AB13	VSS	AC18	VSS
Y4	VDDQ	AA9	VDD18	AB14	VDDA	AC19	VDDA
Y5	M0_SA_CA9	AA10	VSS	AB15	VSS	AC20	VSS
Y6	VSS	AA11	VDDHA	AB16	VDDA	AC21	VDDA
Y7	M0_SA_CA7/M0_SA_DPAR	AA12	VSS	AB17	VSS	AC22	VSS
Y8	M0_SA_CA5	AA13	VDDHA	AB18	VDDA	AC23	HSA1
Y9	VSS	AA14	VSS	AB19	VSS	AC24	HSA2
Y10	VDD18	AA15	VDDHA	AB20	VDDA	AC25	I2C_SCL
Y11	VSS	AA16	VSS	AB21	VSS	AC26	I2C_SDA
Y12	VDDHA	AA17	VDDHA	AB22	VDDA	AC27	I2C_SRSTB
Y13	VSS	AA18	VSS	AB23	HSA0	AC28	M1_SA_DQ16
Y14	VDDHA	AA19	VDDHA	AB24	M1_SA_CS0_n	AC29	VSS
Y15	VSS	AA20	VSS	AB25	M1_SA_CS1_n	AC30	M1_SA_DQ19
Y16	VDDHA	AA21	VDDHA	AB26	VSS	AC31	M1_SA_DQ18
Y17	VSS	AA22	VSS	AB27	M1_SA_CS2_n	AD1	M0_SA_DQ14
Y18	VDDHA	AA23	VDD18	AB28	VDDQ	AD2	M0_SA_DQ13
Y19	VSS	AA24	M1_SA_CS3_n	AB29	M1_SA_DQ17	AD3	M0_SA_DQ12
Y20	VDDHA	AA25	VSS	AB30	M1_SA_DQS2_c	AD4	VDDQ
Y21	VSS	AA26	M1_SA_CA1	AB31	M1_SA_DQS2_t	AD5	TDO
Y22	VDD18	AA27	M1_SA_CA3	AC1	M0_SA_DQ18	AD6	TCK
Y23	VSS	AA28	M1_SA_DQ23	AC2	M0_SA_DQ19	AD7	TMS

Table 49 — Reference #5 DDR5 Use Case Ball Name to Number List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
AD8	VSS	AE13	PETX5_n	AF18	PETX9_p	AG23	PETX14_p
AD9	VSS	AE14	VSS	AF19	PETX10_n	AG24	VSS
AD10	VSS	AE15	PETX7_n	AF20	PETX11_p	AG25	VSS
AD11	VSS	AE16	VSS	AF21	PETX12_n	AG26	PERST0_n
AD12	VSS	AE17	VSS	AF22	PETX13_p	AG27	PERST1_n
AD13	VSS	AE18	PETX9_n	AF23	PETX14_n	AG28	M1_SA_DQ8
AD14	VSS	AE19	VSS	AF24	PETX15_p	AG29	VSS
AD15	VSS	AE20	PETX11_n	AF25	VSS	AG30	M1_SA_DQ11
AD16	VSS	AE21	VSS	AF26	PERES0	AG31	M1_SA_DQ10
AD17	VSS	AE22	PETX13_n	AF27	PERES1	AH1	M0_SA_DQ6
AD18	VSS	AE23	VSS	AF28	VDDQ	AH2	M0_SA_DQ5
AD19	VSS	AE24	PETX15_n	AF29	M1_SA_DQ9	AH3	M0_SA_DQ4
AD20	VSS	AE25	VSS	AF30	M1_SA_DQS1_c	AH4	VDDQ
AD21	VSS	AE26	DUALPORTEN_n	AF31	M1_SA_DQS1_t	AH5	VSS
AD22	VSS	AE27	TXD	AG1	M0_SA_DQ10	AH6	PECLK0_n
AD23	VSS	AE28	M1_SA_DQ15	AG2	M0_SA_DQ11	AH7	VSS
AD24	VSS	AE29	VSS	AG3	VSS	AH8	VSS
AD25	VSS	AE30	M1_SB_DQS1_c	AG4	M0_SA_DQ8	AH9	VSS
AD26	CLKREQ_n	AE31	M1_SB_DQS1_t	AG5	VSS	AH10	VSS
AD27	RXD	AF1	M0_SA_DQS1_t	AG6	REFCLK_p	AH11	VSS
AD28	VDDQ	AF2	M0_SA_DQS1_c	AG7	VSS	AH12	VSS
AD29	M1_SA_DQ12	AF3	M0_SA_DQ9	AG8	PETX0_p	AH13	VSS
AD30	M1_SA_DQ13	AF4	VDDQ	AG9	VSS	AH14	VSS
AD31	M1_SA_DQ14	AF5	VSS	AG10	PETX2_p	AH15	VSS
AE1	M0_SB_DQS1_t	AF6	REFCLK_n	AG11	VSS	AH16	VSS
AE2	M0_SB_DQS1_c	AF7	VSS	AG12	PETX4_p	AH17	VSS
AE3	VSS	AF8	PETX0_n	AG13	VSS	AH18	VSS
AE4	M0_SA_DQ15	AF9	PETX1_p	AG14	PETX6_p	AH19	VSS
AE5	VSS	AF10	PETX2_n	AG15	VSS	AH20	VSS
AE6	VSS	AF11	PETX3_p	AG16	VSS	AH21	VSS
AE7	VSS	AF12	PETX4_n	AG17	PETX8_p	AH22	VSS
AE8	VSS	AF13	PETX5_p	AG18	VSS	AH23	VSS
AE9	PETX1_n	AF14	PETX6_n	AG19	PETX10_p	AH24	VSS
AE10	VSS	AF15	PETX7_p	AG20	VSS	AH25	VSS
AE11	PETX3_n	AF16	VSS	AG21	PETX12_p	AH26	RSVD_DO_NOT_CONNECT
AE12	VSS	AF17	PETX8_n	AG22	VSS	AH27	RSVD_DO_NOT_CONNECT

Table 49 — Reference #5 DDR5 Use Case Ball Name to Number List (cont'd)

No.	Name	No.	Name	No.	Name
AH28	VDDQ	AK2	M0_SA_DQS0_c	AL7	VSS
AH29	M1_SA_DQ4	AK3	M0_SA_DQ1	AL8	PERX0_n
AH30	M1_SA_DQ5	AK4	VDDQ	AL10	PERX2_n
AH31	M1_SA_DQ6	AK5	VSS	AL11	VSS
AJ1	M0_SB_DQS0_t	AK6	PECLK1_n	AL12	PERX4_p
AJ2	M0_SB_DQS0_c	AK7	VSS	AL14	PERX6_p
AJ3	VSS	AK8	PERX0_p	AL16	VSS
AJ4	M0_SA_DQ7	AK9	PERX1_n	AL17	PERX8_n
AJ5	VSS	AK10	PERX2_p	AL19	PERX10_n
AJ6	PECLK0_t	AK11	PERX3_n	AL20	VSS
AJ7	VSS	AK12	PERX4_n	AL21	PERX12_p
AJ8	VSS	AK13	PERX5_p	AL23	PERX14_p
AJ9	PERX1_p	AK14	PERX6_n	AL25	VSS
AJ10	VSS	AK15	PERX7_p	AL26	SCLK
AJ11	PERX3_p	AK16	VSS	AL27	SIO0
AJ12	VSS	AK17	PERX8_p	AL28	M1_SA_DQ0
AJ13	PERX5_n	AK18	PERX9_n	AL29	M1_SA_DQ3
AJ14	VSS	AK19	PERX10_p	AL30	M1_SA_DQ2
AJ15	PERX7_n	AK20	PERX11_n	AL31	VSS
AJ16	VSS	AK21	PERX12_n		
AJ17	VSS	AK22	PERX13_p		
AJ18	PERX9_p	AK23	PERX14_n		
AJ19	VSS	AK24	PERX15_p		
AJ20	PERX11_p	AK25	VSS		
AJ21	VSS	AK26	SCS_n		
AJ22	PERX13_n	AK27	SIO1		
AJ23	VSS	AK28	VDDQ		
AJ24	PERX15_n	AK29	M1_SA_DQ1		
AJ25	VSS	AK30	M1_SA_DQS0_c		
AJ26	SIO2	AK31	M1_SA_DQS0_t		
AJ27	SIO3	AL1	VSS		
AJ28	M1_SA_DQ7	AL2	M0_SA_DQ2		
AJ29	VSS	AL3	M0_SA_DQ3		
AJ30	M1_SB_DQS0_c	AL4	M0_SA_DQ0		
AJ31	M1_SB_DQS0_t	AL5	VSS		
AK1	M0_SA_DQS0_t	AL6	PECLK1_t		

12.3 Reference #6 DDR4 Use Case Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31				
A	VSS	M0_DQS 5,1	VSS	VSS	M0_DQS 15,1	M0_DQ4 6	VSS	M0_DQS 0	M0_DQS 6,1	M0_DQS 16,1	M0_DQS 4	M0_DQS 8	M0_DQS 7,1	M0_DQS 17,1	M0_DQ6 2	VSS	M1_DQS 2	M1_DQS 17,1	M1_DQS 7,1	M1_DQS 8	M1_DQS 4	M1_DQS 16,1	M1_DQS 6,1	M1_DQS 0	VSS	M1_DQ4 6	M1_DQS 15,1	VSS	VSS	M1_DQS 5,1	VSS				
B	M0_DQ4 2	M0_DQS 5,1	M0_DQ4 1	VDDQ	M0_DQS 15,1	M0_DQ4 5	VSS	M0_DQS 1	M0_DQS 6,1	M0_DQS 16,1	M0_DQS 3	M0_DQS 9	M0_DQS 7,1	M0_DQS 17,1	M0_DQ6 1	VSS	M1_DQ6 1	M1_DQS 17,1	M1_DQS 7,1	M1_DQS 9	M1_DQS 3	M1_DQS 16,1	M1_DQS 6,1	M1_DQS 1	VSS	M1_DQ4 5	M1_DQS 15,1	VDDQ	M1_DQ4 1	M0_DQS 5,1	M1_DQ4 2				
C	M0_DQ4 3	VSS	M0_DQ4 0	VSS	VDDQ	M0_DQ4 4	VSS	VSS	M0_DQ4 9	VSS	M0_DQS 2	VSS	M0_DQS 7	VSS	M0_DQ6 0	VSS	M1_DQ6 0	VSS	M1_DQS 7	VSS	M1_DQS 2	VSS	M1_DQ4 9	VSS	VSS	M1_DQ4 4	VDDQ	VSS	M1_DQ4 0	VSS	M1_DQ4 3				
D	M0_DQ3 8	M0_DQ3 7	M0_DQ3 6	VDDQ	M0_DQ4 7	VDDQ	VSS	M0_DQ4 8	VDDQ	M0_DQS 5	VDDQ	M0_DQS 6	VDDQ	M0_DQ6 3	VDDQ	VSS	VDDQ	M1_DQS 3	VDDQ	M1_DQS 6	M1_DQS 5	VDDQ	M1_DQS 8	VSS	VDDQ	M1_DQ4 7	VDDQ	M1_DQ3 6	M1_DQ3 7	M1_DQ3 8					
E	M0_DQS 14,1	M0_DQS 14,1	VSS	M0_DQ3 9	M0_ODT 2	VSS	M0_ODT 1	M0_ODT 0	M0_RESE T_n	M0_ZQ AL	RSVD_D O_NOT_ CONNEC T	RSVD_D O_NOT_ CONNEC T	NC	BOOTSEL 0	BOOTSEL 1	RSTSEL0	RSTSEL1	THERM_ PAD0	NC	RSVD_D O_NOT_ CONNEC T	RSVD_D O_NOT_ CONNEC T	M1_ZQ AL	M1_RESE T_n	M1_ODT 0	M1_ODT 1	VSS	M1_ODT 2	M1_DQ3 9	VSS	M1_DQS 14,1	M1_DQS 14,1				
F	M0_DQS 4,1	M0_DQS 4,1	M0_DQ3 3	VDDQ	M0_A17	M0_CS1 n	VSS	M0_ODT 3	M0_EVE NT_n	VSS	NC	NC	VSS	SAVE_N	CLKSEL	VSS	PWRDVS	THERM_ PAD0	VSS	NC	NC	VSS	M1_EVE NT_n	M1_ODT 3	VSS	M1_CS1 n	M1_A17	VDDQ	M1_DQ3 3	M1_DQS 4,1	M1_DQS 4,1				
G	M0_DQ3 4	M0_DQ3 5	VSS	M0_DQ3 2	M0_CAS n/M0_A1 5	VSS	M0_PAS n/M0_A1 6	M0_CID1	M0_Vref CA	LED1	LED2	RCVRY	NC	FAIL_N	VDD18	GPI07	VDD18	GPI06	NC	GPI05	GPI04	GPI03	M1_Vref CA	M1_CID1	M1_PAS n/M0_A1 6	VSS	M0_CAS n/M0_A1 5	M1_DQ3 2	VSS	M1_DQS 5	M1_DQ3 4				
H	NC	NC	NC	VDDQ	M0_PAR	M0_BA0	VSS	M0_CS3 n	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDD18	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	M1_CS3 n	VSS	M1_BA0	NC	VDDQ	NC	NC	NC
J	NC	NC	VSS	NC	VSS	VSS	M0_CID0	M0_CS0 n	LED0	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	GPI02	M1_CS0 n	M1_CID0	VSS	VSS	NC	VSS	NC	NC		
K	M0_DQS 9,1	M0_DQS 9,1	NC	VDDQ	M0_CK0 c	VSS	M0_CK0 c	VSS	M0_CID0	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDD18	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	M1_CID0	VSS	M1_CK0 c	M1_CK0 c	VDDQ	NC	M1_DQS 9,1	M1_DQS 9,1	
L	NC	NC	VSS	NC	VSS	VSS	M0_WE n/M0_A1 4	M0_AP/ M0_A10	DEBUG3	VSS	VDDQ	VSS	VDDQ	VSS	VSS	VSS	VSS	VDDC	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	GPI01	NC	M1_WE n/M0_A1 4	VSS	VSS	NC	VSS	NC	NC	
M	M0_C86	M0_C85	M0_C84	VDDQ	M0_CK0 c	VSS	M0_CK0 c	VSS	M0_A13	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VDD18	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	VSS	M1_A13	VSS	M1_CK0 c	M1_CK0 c	VDDQ	M1_C84	M1_C85	M1_C86		
N	NC	NC	VSS	M0_C87	VSS	VSS	M0_A0	M0_CS2 n	DEBUG2	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	GPI00	M1_CS2 n	M1_A0	VSS	VSS	M1_C87	VSS	NC	NC		
P	M0_DQS 8,1	M0_DQS 8,1	M0_C81	VDDQ	VSS	VSS	M0_A4	M0_ALER T_n	VSS	VDDQ	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	VSS	M1_ALER T_n	M1_A4	VSS	VSS	VDDQ	M1_C81	M1_DQS 8,1	M1_DQS 8,1			
R	M0_C82	M0_C83	VSS	M0_C80	M0_CK1 c	VSS	M0_CK1 c	VSS	M0_A1	DEBUG1	VSS	VDDQ	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDA	VSS	VDDQ	VSS	VDDQ	VSS	EVENT_N	M1_A1	VSS	M1_CK1 c	M1_CK1 c	M1_C80	VSS	M1_C82		
T	M0_DQ3 0	M0_DQ3 9	M0_DQ2 8	VDDQ	VSS	VSS	M0_A3	M0_A6	VSS	VDDQ	VSS	VDDC	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	VDDQ	VSS	M1_A6	M1_A3	VSS	VSS	VDDQ	M1_DQ2 8	M1_DQ3 9	M1_DQ3 0
U	M0_DQS 13,1	M0_DQS 13,1	VSS	M0_DQ1 1	M0_CK0 c	VSS	M0_CK0 c	VSS	M0_A7	DEBUG0	VSS	VDDQ	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDQ	VSS	VSS	M1_SCAN _PCAP_5 EL	M1_A7	VSS	M1_CK0 c	M1_CK0 c	M1_DQ1 1	VSS	M1_DQS 13,1	M1_DQS 13,1		
V	M0_DQS 3,1	M0_DQS 3,1	M0_DQ2 5	VDDQ	VSS	VSS	M0_ACT n/M0_A1 2	VSS	RSVD_D O_NOT_ CONNEC T	RSVD_D O_NOT_ CONNEC T	VSS	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDD10	VSS	MSDA	HSCL	M1_ACT n	NC	VSS	VSS	VDDQ	M1_DQ2 5	M1_DQS 3,1	M1_DQS 3,1			
W	M0_DQ2 6	M0_DQ2 7	VSS	M0_DQ2 4	M0_BA1	M0_A2	VSS	M0_BG0	VDD18	VSS	VDDA	VSS	VDDA	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDDC	VSS	VDD18	MSCL	HSDA	M1_BG0	VSS	M1_A2	M1_BA1	M1_DQ2 4	VSS	M1_DQ2 6			
Y	M0_DQ2 2	M0_DQ2 1	M0_DQ2 0	VDDQ	M0_A5	VSS	M0_A8	M0_A11	VSS	VDD18	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDD18	VSS	M1_A11	M1_A8	VSS	M1_A5	VDDQ	M1_DQ2 0	M1_DQ2 1	M1_DQ2 2		
AA	M0_DQS 12,1	M0_DQS 12,1	VSS	M0_DQ2 3	M0_A9	M0_BG1	VSS	M0_CK0	VDD18	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDDHA	VSS	VDD18	VSS	VDD18	M1_CK0	VSS	M1_BG1	M1_A9	M1_DQ2 3	VSS	M1_DQS 12,1	M1_DQS 12,1		
AB	M0_DQS 2,1	M0_DQS 2,1	M0_DQ1 7	VDDQ	M0_CK2	VSS	M0_CK1	M0_CK0	PGOOD/ RESET_n	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	HS40	M1_CK0	M1_CK1	VSS	M1_CK2	VDDQ	M1_DQ1 7	M1_DQS 2,1	M1_DQS 2,1		
AC	M0_DQ1 8	M0_DQ1 9	VSS	M0_DQ1 6	TRST_n	TAP_SEL	TDI	TMUXSEL 0	TMUXSEL 1	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	VDDA	VSS	HS41	HS42	IC2_SCL	IC2_SDA	IC2_SRT B	M1_DQ1 6	VSS	M1_DQ1 8	M1_DQ1 9		
AD	M0_DQ1 4	M0_DQ1 3	M0_DQ1 2	VDDQ	TDO	TCK	TMS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		
AE	M0_DQS 11,1	M0_DQS 11,1	VSS	M0_DQ1 5	VSS	VSS	VSS	PETX1_n	VSS	PETX3_n	VSS	PETX5_n	VSS	PETX7_n	VSS	VSS	VSS	PETX9_n	VSS	VSS	PETX10_n	VSS	PETX11_n	VSS	PETX13_n	VSS	PETX15_n	VSS	DUALPO RTEN_n	TXD	M1_DQ1 5	VSS	M1_DQS 11,1	M1_DQS 11,1	
AF	M0_DQS 1,1	M0_DQS 1,1	M0_DQ9	VDDQ	VSS	REFCLK_n	VSS	PETX0_n	VSS	PETX1_p	VSS	PETX2_p	VSS	PETX4_p	VSS	PETX6_p	VSS	PETX8_p	VSS	PETX9_p	VSS	PETX10_p	VSS	PETX11_p	VSS	PETX12_p	VSS	PETX13_p	VSS	PETX14_p	VSS	PETX15_p	VSS	PETX16_p	
AG	M0_DQ1 0	M0_DQ1 1	VSS	M0_DQ8	VSS	REFCLK_p	VSS	PETX0_p	VSS	PETX1_p	VSS	PETX2_p	VSS	PETX4_p	VSS	PETX6_p	VSS	PETX8_p	VSS	PETX9_p	VSS	PETX10_p	VSS	PETX11_p	VSS	PETX12_p	VSS	PETX13_p	VSS	PETX14_p	VSS	PETX15_p	VSS	PETX16_p	
AH	M0_DQ6	M0_DQS	M0_DQ4	VDDQ	VSS	PECLK0_n	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		
AJ	M0_DQS 10,1	M0_DQS 10,1	VSS	M0_DQ7	VSS	PECLK0,1	VSS	VSS	PERX1_p	VSS	PERX3_p	VSS	PERX5_n	VSS	PERX7_n	VSS	VSS	PERX9_p	VSS	VSS	PERX10_p	VSS	PERX11_p	VSS	PERX13_n	VSS	PERX15_n	VSS	SIO2	M1_DQ7	VSS	M1_DQS 10,1	M1_DQS 10,1		
AK	M0_DQS 0,1	M0_DQS 0,1	M0_DQ1	VDDQ	VSS	PECLK1_n	VSS	PERX0_p	VSS	PERX1_n	VSS	PERX2_p	VSS	PERX4_p	VSS	PERX6_p	VSS	PERX8_p	VSS	PERX9_p	VSS	PERX10_p	VSS	PERX11_p	VSS	PERX12_p	VSS	PERX13_p	VSS	PERX14_p	VSS	PERX15_p	VSS	PERX16_p	
AL	VSS	M0_DQ2	M0_DQ3	M0_DQ0	VSS	PECLK1,1	VSS	PERX0_n	VSS	PERX2_n	VSS	PERX4_p	VSS	PERX6_p	VSS	VSS	PERX8_p	VSS	VSS	PERX9_p	VSS	PERX10_p	VSS	PERX11_p	VSS	PERX12_p	VSS	PERX13_p	VSS	PERX14_p	VSS	PERX15_p	VSS	PERX16_p	

Figure 16 — Reference #6 DDR4 Use Case Ball Map

12.3 Reference #6 DDR4 Use Case Ball Map (cont'd)**Table 50 — Reference #6 DDR4 Use Case Ball Number to Name List**

No.	Name	No.	Name	No.	Name	No.	Name
A1	VSS	B6	M0_DQ45	C11	M0_DQ52	D16	VSS
A2	M0_DQS5_t	B7	VSS	C12	VSS	D17	VDDQ
A3	VSS	B8	M0_DQ51	C13	M0_DQ57	D18	M1_DQ63
A4	VSS	B9	M0_DQS6_c	C14	VSS	D19	VDDQ
A5	M0_DQS15_t	B10	M0_DQS16_c	C15	M0_DQ60	D20	M1_DQ56
A6	M0_DQ46	B11	M0_DQ53	C16	VSS	D21	VDDQ
A7	VSS	B12	M0_DQ59	C17	M1_DQ60	D22	M1_DQ55
A8	M0_DQ50	B13	M0_DQS7_c	C18	VSS	D23	VDDQ
A9	M0_DQS6_t	B14	M0_DQS17_c	C19	M1_DQ57	D24	M1_DQ48
A10	M0_DQS16_t	B15	M0_DQ61	C20	VSS	D25	VSS
A11	M0_DQ54	B16	VSS	C21	M1_DQ52	D26	VDDQ
A12	M0_DQ58	B17	M1_DQ61	C22	VSS	D27	M1_DQ47
A13	M0_DQS7_t	B18	M1_DQS17_c	C23	M1_DQ49	D28	VDDQ
A14	M0_DQS17_t	B19	M1_DQS7_c	C24	VSS	D29	M1_DQ36
A15	M0_DQ62	B20	M1_DQ59	C25	VSS	D30	M1_DQ37
A16	VSS	B21	M1_DQ53	C26	M1_DQ44	D31	M1_DQ38
A17	M1_DQ62	B22	M1_DQS16_c	C27	VDDQ	E1	M0_DQS14_t
A18	M1_DQS17_t	B23	M1_DQS6_c	C28	VSS	E2	M0_DQS14_c
A19	M1_DQS7_t	B24	M1_DQ51	C29	M1_DQ40	E3	VSS
A20	M1_DQ58	B25	VSS	C30	VSS	E4	M0_DQ39
A21	M1_DQ54	B26	M1_DQ45	C31	M1_DQ43	E5	M0_ODT2
A22	M1_DQS16_t	B27	M1_DQS15_c	D1	M0_DQ38	E6	VSS
A23	M1_DQS6_t	B28	VDDQ	D2	M0_DQ37	E7	M0_ODT1
A24	M1_DQ50	B29	M1_DQ41	D3	M0_DQ36	E8	M0_ODT0
A25	VSS	B30	M1_DQS5_c	D4	VDDQ	E9	M0_RESET_n
A26	M1_DQ46	B31	M1_DQ42	D5	M0_DQ47	E10	M0_ZQCAL
A27	M1_DQS15_t	C1	M0_DQ43	D6	VDDQ	E11	RSVD_DO_NOT_CONNECT
A28	VSS	C2	VSS	D7	VSS	E12	RSVD_DO_NOT_CONNECT
A29	VSS	C3	M0_DQ40	D8	M0_DQ48	E13	NC
A30	M1_DQS5_t	C4	VSS	D9	VDDQ	E14	BOOTSEL0
A31	VSS	C5	VDDQ	D10	M0_DQ55	E15	BOOTSEL1
B1	M0_DQ42	C6	M0_DQ44	D11	VDDQ	E16	RSTSEL0
B2	M0_DQS5_c	C7	VSS	D12	M0_DQ56	E17	RSTSEL1
B3	M0_DQ41	C8	VSS	D13	VDDQ	E18	THERM_PADB
B4	VDDQ	C9	M0_DQ49	D14	M0_DQ63	E19	NC
B5	M0_DQS15_c	C10	VSS	D15	VDDQ	E20	RSVD_DO_NOT_CONNECT

Table 50 — Reference #6 DDR4 Use Case Ball Number to Name List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
E21	RSVD_DO_NOT_CONNECT	F26	M1_CS1_n	G31	M1_DQ34	J5	VSS
E22	M1_ZQCAL	F27	M1_A17	H1	NC	J6	VSS
E23	M1_RESET_n	F28	VDDQ	H2	NC	J7	M0_CID2
E24	M1_ODT0	F29	M1_DQ33	H3	NC	J8	M0_CS0_n
E25	M1_ODT1	F30	M1_DQS4_c	H4	VDDQ	J9	LED0
E26	VSS	F31	M1_DQS4_t	H5	M0_PAR	J10	VSS
E27	M1_ODT2	G1	M0_DQ34	H6	M0_BA0	J11	VDDQ
E28	M1_DQ39	G2	M0_DQ35	H7	VSS	J12	VSS
E29	VSS	G3	VSS	H8	M0_CS3_n	J13	VDDQ
E30	M1_DQS14_c	G4	M0_DQ32	H9	VSS	J14	VSS
E31	M1_DQS14_t	G5	M0_CAS_n/M0_A15	H10	VDDQ	J15	VDDQ
F1	M0_DQS4_t	G6	VSS	H11	VSS	J16	VSS
F2	M0_DQS4_c	G7	M0_RAS_n/M0_A16	H12	VDDQ	J17	VDDQ
F3	M0_DQ33	G8	M0_CID1	H13	VSS	J18	VSS
F4	VDDQ	G9	M0_VrefCA	H14	VDDQ	J19	VDDQ
F5	M0_A17	G10	LED1	H15	VSS	J20	VSS
F6	M0_CS1_n	G11	LED2	H16	VDD18	J21	VDDQ
F7	VSS	G12	RCVRY	H17	VSS	J22	VSS
F8	M0_ODT3	G13	NC	H18	VDDQ	J23	GPIO2
F9	M0_EVENT_n	G14	FAIL_N	H19	VSS	J24	M1_CS0_n
F10	VSS	G15	VDD18	H20	VDDQ	J25	M1_CID2
F11	NC	G16	GPIO7	H21	VSS	J26	VSS
F12	NC	G17	VDD18	H22	VDDQ	J27	VSS
F13	VSS	G18	GPIO6	H23	VSS	J28	NC
F14	SAVE_N	G19	NC	H24	M1_CS3_n	J29	VSS
F15	CLKSEL	G20	GPIO5	H25	VSS	J30	NC
F16	VSS	G21	GPIO4	H26	M1_BA0	J31	NC
F17	PWRDIS	G22	GPIO3	H27	NC	K1	M0_DQS9_t
F18	THERM_PADE	G23	M1_VrefCA	H28	VDDQ	K2	M0_DQS9_c
F19	VSS	G24	M1_CID1	H29	NC	K3	NC
F20	NC	G25	M1_RAS_n/M1_A16	H30	NC	K4	VDDQ
F21	NC	G26	VSS	H31	NC	K5	M0_CKC_c
F22	VSS	G27	M1_CAS_n/M1_A15	J1	NC	K6	M0_CKC_t
F23	M1_EVENT_n	G28	M1_DQ32	J2	NC	K7	VSS
F24	M1_ODT3	G29	VSS	J3	VSS	K8	M0_CID0
F25	VSS	G30	M1_DQ35	J4	NC	K9	VSS

Table 50 — Reference #6 DDR4 Use Case Ball Number to Name List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
K10	VDDQ	L15	VSS	M20	VDDC	N25	M1_A0
K11	VSS	L16	VSS	M21	VSS	N26	VSS
K12	VDDQ	L17	VDDC	M22	VDDQ	N27	VSS
K13	VSS	L18	VSS	M23	VSS	N28	M1_CB7
K14	VDDQ	L19	VDDQ	M24	M1_A13	N29	VSS
K15	VSS	L20	VSS	M25	VSS	N30	NC
K16	VDD18	L21	VDDQ	M26	M1_CKD_c	N31	NC
K17	VSS	L22	VSS	M27	M1_CKC_t	P1	M0_DQS8_t
K18	VDDQ	L23	GPIO1	M28	VDDQ	P2	M0_DQS8_c
K19	VSS	L24	NC	M29	M1_CB4	P3	M0_CB1
K20	VDDQ	L25	M1_WE_n/M1_A14	M30	M1_CB5	P4	VDDQ
K21	VSS	L26	VSS	M31	M1_CB6	P5	VSS
K22	VDDQ	L27	VSS	N1	NC	P6	VSS
K23	VSS	L28	NC	N2	NC	P7	M0_A4
K24	M1_CID0	L29	VSS	N3	VSS	P8	M0_ALERT_n
K25	VSS	L30	NC	N4	M0_CB7	P9	VSS
K26	M1_CKC_c	L31	NC	N5	VSS	P10	VDDQ
K27	" M1_CKD_t"	M1	M0_CB6	N6	VSS	P11	VSS
K28	VDDQ	M2	M0_CB5	N7	M0_A0	P12	VDDC
K29	NC	M3	M0_CB4	N8	" M0_CS2_n"	P13	VSS
K30	M1_DQS9_c	M4	VDDQ	N9	DEBUG2	P14	VDDC
K31	M1_DQS9_t	M5	M0_CKD_c	N10	VSS	P15	VSS
L1	NC	M6	M0_CKD_t	N11	VDDQ	P16	VDDC
L2	NC	M7	VSS	N12	VSS	P17	VSS
L3	VSS	M8	M0_A13	N13	VDDC	P18	VDDC
L4	NC	M9	VSS	N14	VSS	P19	VSS
L5	VSS	M10	VDDQ	N15	VDDC	P20	VDDC
L6	VSS	M11	VSS	N16	VSS	P21	VSS
L7	M0_WE_n/M0_A14	M12	VDDC	N17	VDDC	P22	VDDQ
L8	M0_AP/M0_A10	M13	VSS	N18	VSS	P23	VSS
L9	DEBUG3	M14	VDDC	N19	VDDC	P24	M1_ALERT_n
L10	VSS	M15	VSS	N20	VSS	P25	M1_A4
L11	VDDQ	M16	VDD18	N21	VDDQ	P26	VSS
L12	VSS	M17	VSS	N22	VSS	P27	VSS
L13	VDDQ	M18	VDDC	N23	GPIO0	P28	VDDQ
L14	VSS	M19	VSS	N24	" M1_CS2_n"	P29	M1_CB1

Table 50 — Reference #6 DDR4 Use Case Ball Number to Name List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
P30	M1_DQS8_c	T4	VDDQ	U9	DEBUG0	V14	VDDA
P31	M1_DQS8_t	T5	VSS	U10	VSS	V15	VSS
R1	M0_CB2	T6	VSS	U11	VDDQ	V16	VDDC
R2	M0_CB3	T7	M0_A3	U12	VSS	V17	VSS
R3	VSS	T8	M0_A6	U13	VDDA	V18	VDDC
R4	M0_CB0	T9	VSS	U14	VSS	V19	VSS
R5	M0_CKA_c	T10	VDDQ	U15	VDDC	V20	VDD10
R6	M0_CKA_t	T11	VSS	U16	VSS	V21	VSS
R7	VSS	T12	VDDC	U17	VDDC	V22	MSDA
R8	M0_A1	T13	VSS	U18	VSS	V23	HSCL
R9	DEBUG1	T14	VDDA	U19	VDDC	V24	M1_ACT_n
R10	VSS	T15	VSS	U20	VSS	V25	NC
R11	VDDQ	T16	VDDC	U21	VDDQ	V26	VSS
R12	VSS	T17	VSS	U22	VSS	V27	VSS
R13	VDDA	T18	VDDC	U23	M_SCAN_PCAP_SEL	V28	VDDQ
R14	VSS	T19	VSS	U24	M1_A7	V29	M1_DQ25
R15	VDDC	T20	VDDC	U25	VSS	V30	M1_DQS3_c
R16	VSS	T21	VSS	U26	M1_CKB_t	V31	M1_DQS3_t
R17	VDDC	T22	VDDQ	U27	M1_CKB_c	W1	M0_DQ26
R18	VSS	T23	VSS	U28	M1_DQ31	W2	M0_DQ27
R19	VDDA	T24	M1_A6	U29	VSS	W3	VSS
R20	VSS	T25	M1_A3	U30	M1_DQS13_c	W4	M0_DQ24
R21	VDDQ	T26	VSS	U31	M1_DQS13_t	W5	M0_BA1
R22	VSS	T27	VSS	V1	M0_DQS3_t	W6	M0_A2
R23	EVENT_N	T28	VDDQ	V2	M0_DQS3_c	W7	VSS
R24	M1_A1	T29	M1_DQ28	V3	M0_DQ25	W8	M0_BG0
R25	VSS	T30	M1_DQ29	V4	VDDQ	W9	VDD18
R26	M1_CKA_t	T31	M1_DQ30	V5	VSS	W10	VSS
R27	M1_CKA_c	U1	M0_DQS13_t	V6	VSS	W11	VDDA
R28	M1_CB0	U2	M0_DQS13_c	V7	M0_BC_n/M0_A12	W12	VSS
R29	VSS	U3	VSS	V8	M0_ACT_n	W13	VDDA
R30	M1_CB3	U4	M0_DQ31	V9	VSS	W14	VSS
R31	M1_CB2	U5	M0_CKB_c	V10	RSVD_DO_NOT_CONNECT	W15	VDDC
T1	M0_DQ30	U6	M0_CKB_t	V11	RSVD_DO_NOT_CONNECT	W16	VSS
T2	M0_DQ29	U7	VSS	V12	VDDC	W17	VDDC
T3	M0_DQ28	U8	M0_A7	V13	VSS	W18	VSS

Table 50 — Reference #6 DDR4 Use Case Ball Number to Name List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
W19	VDDC	Y24	M1_A11	AA29	VSS	AC3	VSS
W20	VSS	Y25	M1_A8	AA30	M1_DQS12_c	AC4	M0_DQ16
W21	VDD18	Y26	VSS	AA31	M1_DQS12_t	AC5	TRST_n
W22	MSCL	Y27	M1_A5	AB1	M0_DQS2_t	AC6	TAP_SEL
W23	HSDA	Y28	VDDQ	AB2	M0_DQS2_c	AC7	TDI
W24	M1_BG0	Y29	M1_DQ20	AB3	M0_DQ17	AC8	TMUXSEL0
W25	VSS	Y30	M1_DQ21	AB4	VDDQ	AC9	TMUXSEL1
W26	M1_A2	Y31	M1_DQ22	AB5	M0_CKE2	AC10	VSS
W27	M1_BA1	AA1	M0_DQS12_t	AB6	VSS	AC11	VDDA
W28	M1_DQ24	AA2	M0_DQS12_c	AB7	M0_CKE1	AC12	VSS
W29	VSS	AA3	VSS	AB8	M0_CKE0	AC13	VDDA
W30	M1_DQ27	AA4	M0_DQ23	AB9	PGOOD / RESET_n	AC14	VSS
W31	M1_DQ26	AA5	M0_A9	AB10	VDDA	AC15	VDDA
Y1	M0_DQ22	AA6	M0_BG1	AB11	VSS	AC16	VSS
Y2	M0_DQ21	AA7	VSS	AB12	VDDA	AC17	VDDA
Y3	M0_DQ20	AA8	M0_CKE3	AB13	VSS	AC18	VSS
Y4	VDDQ	AA9	VDD18	AB14	VDDA	AC19	VDDA
Y5	M0_A5	AA10	VSS	AB15	VSS	AC20	VSS
Y6	VSS	AA11	VDDHA	AB16	VDDA	AC21	VDDA
Y7	M0_A8	AA12	VSS	AB17	VSS	AC22	VSS
Y8	M0_A11	AA13	VDDHA	AB18	VDDA	AC23	HSA1
Y9	VSS	AA14	VSS	AB19	VSS	AC24	HSA2
Y10	VDD18	AA15	VDDHA	AB20	VDDA	AC25	I2C_SCL
Y11	VSS	AA16	VSS	AB21	VSS	AC26	I2C_SDA
Y12	VDDHA	AA17	VDDHA	AB22	VDDA	AC27	I2C_SRSTB
Y13	VSS	AA18	VSS	AB23	HSA0	AC28	M1_DQ16
Y14	VDDHA	AA19	VDDHA	AB24	M1_CKE0	AC29	VSS
Y15	VSS	AA20	VSS	AB25	M1_CKE1	AC30	M1_DQ19
Y16	VDDHA	AA21	VDDHA	AB26	VSS	AC31	M1_DQ18
Y17	VSS	AA22	VSS	AB27	M1_CKE2	AD1	M0_DQ14
Y18	VDDHA	AA23	VDD18	AB28	VDDQ	AD2	M0_DQ13
Y19	VSS	AA24	M1_CKE3	AB29	M1_DQ17	AD3	M0_DQ12
Y20	VDDHA	AA25	VSS	AB30	M1_DQS2_c	AD4	VDDQ
Y21	VSS	AA26	M1_BG1	AB31	M1_DQS2_t	AD5	TDO
Y22	VDD18	AA27	M1_A9	AC1	M0_DQ18	AD6	TCK
Y23	VSS	AA28	M1_DQ23	AC2	M0_DQ19	AD7	TMS

Table 50 — Reference #6 DDR4 Use Case Ball Number to Name List (cont'd)

No.	Name	No.	Name	No.	Name	No.	Name
AD8	VSS	AE13	PETX5_n	AF18	PETX9_p	AG23	PETX14_p
AD9	VSS	AE14	VSS	AF19	PETX10_n	AG24	VSS
AD10	VSS	AE15	PETX7_n	AF20	PETX11_p	AG25	VSS
AD11	VSS	AE16	VSS	AF21	PETX12_n	AG26	PERST0_n
AD12	VSS	AE17	VSS	AF22	PETX13_p	AG27	PERST1_n
AD13	VSS	AE18	PETX9_n	AF23	PETX14_n	AG28	M1_DQ8
AD14	VSS	AE19	VSS	AF24	PETX15_p	AG29	VSS
AD15	VSS	AE20	PETX11_n	AF25	VSS	AG30	M1_DQ11
AD16	VSS	AE21	VSS	AF26	PERES0	AG31	M1_DQ10
AD17	VSS	AE22	PETX13_n	AF27	PERES1	AH1	M0_DQ6
AD18	VSS	AE23	VSS	AF28	VDDQ	AH2	M0_DQ5
AD19	VSS	AE24	PETX15_n	AF29	M1_DQ9	AH3	M0_DQ4
AD20	VSS	AE25	VSS	AF30	M1_DQS1_c	AH4	VDDQ
AD21	VSS	AE26	DUALPORTEN_n	AF31	M1_DQS1_t	AH5	VSS
AD22	VSS	AE27	TXD	AG1	M0_DQ10	AH6	PECLK0_n
AD23	VSS	AE28	M1_DQ15	AG2	M0_DQ11	AH7	VSS
AD24	VSS	AE29	VSS	AG3	VSS	AH8	VSS
AD25	VSS	AE30	M1_DQS11_c	AG4	M0_DQ8	AH9	VSS
AD26	CLKREQ_n	AE31	M1_DQS11_t	AG5	VSS	AH10	VSS
AD27	RXD	AF1	M0_DQS1_t	AG6	REFCLK_p	AH11	VSS
AD28	VDDQ	AF2	M0_DQS1_c	AG7	VSS	AH12	VSS
AD29	M1_DQ12	AF3	M0_DQ9	AG8	PETX0_p	AH13	VSS
AD30	M1_DQ13	AF4	VDDQ	AG9	VSS	AH14	VSS
AD31	M1_DQ14	AF5	VSS	AG10	PETX2_p	AH15	VSS
AE1	M0_DQS11_t	AF6	REFCLK_n	AG11	VSS	AH16	VSS
AE2	M0_DQS11_c	AF7	VSS	AG12	PETX4_p	AH17	VSS
AE3	VSS	AF8	PETX0_n	AG13	VSS	AH18	VSS
AE4	M0_DQ15	AF9	PETX1_p	AG14	PETX6_p	AH19	VSS
AE5	VSS	AF10	PETX2_n	AG15	VSS	AH20	VSS
AE6	VSS	AF11	PETX3_p	AG16	VSS	AH21	VSS
AE7	VSS	AF12	PETX4_n	AG17	PETX8_p	AH22	VSS
AE8	VSS	AF13	PETX5_p	AG18	VSS	AH23	VSS
AE9	PETX1_n	AF14	PETX6_n	AG19	PETX10_p	AH24	VSS
AE10	VSS	AF15	PETX7_p	AG20	VSS	AH25	VSS
AE11	PETX3_n	AF16	VSS	AG21	PETX12_p	AH26	RSVD_DO_NOT_CONNECT
AE12	VSS	AF17	PETX8_n	AG22	VSS	AH27	RSVD_DO_NOT_CONNECT

Table 50 — Reference #6 DDR4 Use Case Ball Number to Name List (cont'd)

No.	Name	No.	Name	No.	Name
AH28	VDDQ	AK2	M0_DQS0_c	AL7	VSS
AH29	M1_DQ4	AK3	M0_DQ1	AL8	PERX0_n
AH30	M1_DQ5	AK4	VDDQ	AL10	PERX2_n
AH31	M1_DQ6	AK5	VSS	AL11	VSS
AJ1	M0_DQS10_t	AK6	PECLK1_n	AL12	PERX4_p
AJ2	M0_DQS10_c	AK7	VSS	AL14	PERX6_p
AJ3	VSS	AK8	PERX0_p	AL16	VSS
AJ4	M0_DQ7	AK9	PERX1_n	AL17	PERX8_n
AJ5	VSS	AK10	PERX2_p	AL19	PERX10_n
AJ6	PECLK0_t	AK11	PERX3_n	AL20	VSS
AJ7	VSS	AK12	PERX4_n	AL21	PERX12_p
AJ8	VSS	AK13	PERX5_p	AL23	PERX14_p
AJ9	PERX1_p	AK14	PERX6_n	AL25	VSS
AJ10	VSS	AK15	PERX7_p	AL26	SCLK
AJ11	PERX3_p	AK16	VSS	AL27	SIO0
AJ12	VSS	AK17	PERX8_p	AL28	M1_DQ0
AJ13	PERX5_n	AK18	PERX9_n	AL29	M1_DQ3
AJ14	VSS	AK19	PERX10_p	AL30	M1_DQ2
AJ15	PERX7_n	AK20	PERX11_n	AL31	VSS
AJ16	VSS	AK21	PERX12_n		
AJ17	VSS	AK22	PERX13_p		
AJ18	PERX9_p	AK23	PERX14_n		
AJ19	VSS	AK24	PERX15_p		
AJ20	PERX11_p	AK25	VSS		
AJ21	VSS	AK26	SCS_n		
AJ22	PERX13_n	AK27	SIO1		
AJ23	VSS	AK28	VDDQ		
AJ24	PERX15_n	AK29	M1_DQ1		
AJ25	VSS	AK30	M1_DQS0_c		
AJ26	SIO2	AK31	M1_DQS0_t		
AJ27	SIO3	AL1	VSS		
AJ28	M1_DQ7	AL2	M0_DQ2		
AJ29	VSS	AL3	M0_DQ3		
AJ30	M1_DQS10_c	AL4	M0_DQ0		
AJ31	M1_DQS10_t	AL5	VSS		
AK1	M0_DQS0_t	AL6	PECLK1_t		

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Standard Improvement Form

JEDEC Standard No. **JESD319**

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